Abstract—Mixed-signal current-mode control (MCMC) implementation has been gaining popularity, because of the tuning flexibility using the digital voltage controller \( G_c(z) \) along with the fast-changing analog current controller. Generally a continuous-time frequency-domain approach is adopted for the design of \( G_c(z) \); however, this method often fails to capture sub-harmonic, more generally the fast-scale instability due to finite discretization effects. This paper derives approximate discrete-time models and proposes a unified framework to derive closed-form stability conditions and discrete-time small-signal models of a synchronous buck converter under MCMC. Considering the effects due to finite output-voltage sampling and the effective series resistance (ESR) of the output capacitor, the stability boundary in MCMC is found to be significantly restricted compared to its analog counterpart. Further, design methods are proposed to enhance stability boundary with improved transient performance by tuning the controller directly in the digital domain. A buck converter prototype is made, and the MCMC technique is realized using an FPGA device. Analytical predictions are verified experimentally.

Index Terms—Mixed-signal, digital current mode control, finite sampling, sub-harmonic instability, discrete-time modeling.

I. INTRODUCTION

RECENT trends in digital power management have been gaining growing interests in mainstream power electronics, particularly for low-to-medium power DC-DC converters [1]. This trend will continue to increase due to their ease of integration with other digital systems, real-time energy optimization [2], [3], ability to implement high performance control schemes [4], [5], immunity to noise and analog component variations, high switching frequency with compact size [6], and faster time-to-market [7].

Controller auto-tuning can achieve fast transient recovery in digitally voltage mode controlled (VMC) DC-DC converters [8]. Current mode control (CMC) can further improve closed-loop bandwidth and stability margin by considering the sensed inductor current loop [9]. This also achieves excellent line regulation and audio-susceptibility [10], compared to VMC. A direct implementation of CMC in a digital pulse width modulated (DPWM) DC-DC converter is difficult to realize, primarily due to fast-changing inductor current with the switching frequency beyond a few hundreds of kHz. Over the last decade, significant research efforts have been attempted to develop simple, cost-effective, and power-efficient digital CMC techniques [11]–[17]. The predictive CMC in [11] and the digital CMC techniques in [12] consider uniform current loop sampling. Such methods can be stabilized over a wide operating range using a combined open/closed-loop technique in [13]. However, due to the limited inductor current samples, high performance control techniques, such as time optimal control [5] are difficult to implement. Mixed signal current mode control (MCMC) considers a mixed-domain approach where the voltage controller is realized in the digital domain, and the current-loop has a traditional analog implementation [17], [18], which is presented below.

A. Mixed-signal current mode control (MCMC)

Figure 1 shows the schematic of a DC-DC synchronous buck converter governed by MCMC [17]. The error voltage \( v_e \) is sampled using an analog-to-digital converter (ADC) at the rate of switching frequency \( F_s \) to generate \( v_e[n] \). The digital voltage controller \( G_c(z) \) is computed at the same rate of \( F_s \). An optional discrete-time ramp \( v_R[n] \) may be considered with the controller output \( v_e[n] \) to stabilize the current-loop for duty ratio \( D > 0.5 \) [18]. The result is then converted into an analog voltage \( v_A \) using a digital-to-analog converter (DAC). Similar to analog CMC, the inductor current \( i_L \) in MCMC is directly compared with \( v_A \) in the analog domain as shown in Fig. 1. The comparator output \( u_c \) follows an RS flip/flop, which is used to generate the respective high-side and low-side gate signals \( u_H \) and \( u_L \), using a dead-time circuit.

B. Existing off-line MCMC controller design with case study

An indirect emulation method is generally adopted for the off-line voltage controller \( G_c(z) \) design under MCMC. Here a continuous-time frequency-domain approach is used to design an equivalent analog controller \( G(s) \) [19]. Thereafter,
a bilinear transformation is used to obtain $G_c(z)$. This method allows the designers to apply well-known frequency domain techniques, which is used in various commercial products [18], [20], [21]. However, depending on the sampling frequency, the zero-order-hold (ZOH) effect may significantly degrade the phase margin. A transformed domain approach can be used to design $G_c(z)$ directly in digital domain and to meet the desired specifications [22], [23]. However, the discrete-time control-to-output transfer function is derived using averaged small-signal models [24] followed by ZOH-equivalent. This ignores the ripple information and fails to predict cycle-by-cycle stability, which is discussed with the following case study.

Consider a nominal parameter set for the buck converter as: $T = 5 \mu s$, $L = 10 \mu H$, $C = 200 \mu F$, $R \in [0.45 \Omega, 2 \Omega]$, $r_c = 45 \Omega$, $v_{in} \in [6, 10] \text{V}$, and $v_{ref} = 3.3 \text{V}$.

Consider $G_c(z)$ in Fig. 1 to be a discrete-time proportional-integral (PI) controller as follows

$$v_c[n] = k_p v_{e}[n] + u_1[n]; \quad u_1[n] = u_1[n-1] + k_i v_{e}[n],$$

(1)

with $v_{e}[n] = (v_{ref} - v_{in})$, where $v_{e}$ and $v_{ref}$ indicate the output voltage and the reference voltage; $k_p$ and $k_i$ are the proportional and integral gains in the discrete domain. For 200 kHz switching frequency, the objective is to achieve 9 kHz closed-loop bandwidth and 70 degree phase margin. Using MATLAB SISO toolbox, the controller parameters in (1) at 8 V input are found to be $k_p = 5$ and $k_i = 0.055$. However, Fig. 2 shows that the MCMC technique exhibits sub-harmonic instability for duty ratio $D = 0.413$, whereas the analog CMC scheme remains stable. Although instability in digital VMC is mainly because of finite quantization [25], the effect of finite output-voltage sampling is primarily responsible for instability in MCMC. This increases ripple parameters [26], thereby increasing conduction loss. A higher $k_p$ using the proximate time optimal tuning in [5] further degrades stability of the buck converter under MCMC, even for $D < 0.5$, and through experimentation, a compensating ramp with a suitable slope is found to be a stabilizing solution.

Stability analysis of analog CMC with the closed voltage-loop was recently reported in [27] which provides closed-form solutions. A ripple-based approach in [28] and the Filippov’s method in [29] present methods for fast-scale stability analysis. Accurate discrete-time models in [30] are useful; however, the main difficulty is to simplify matrix exponential functions to obtain closed-form stability boundary. Thus approximate discrete-time models would be needed for analytical study, and such models in [31], [32] were used to predict fast-scale stability of a ripple-based switching regulator with a reasonable accuracy. However, to the best of our knowledge, the impacts of finite sampling and capacitor’s ESR on the fast-scale stability have not been analyzed so far for uniformly sampled MCMC with the closed voltage-loop.

This paper derives approximate discrete-time models and proposes a unified framework to (i) formulate closed-form stability conditions, (ii) identify methods for enhanced stability boundary, and (iii) derive discrete-time small-signal transfer functions for direct digital controller design to meet the desired specifications. Considering linear slopes of the inductor current and taking into account the capacitor ESR, approximate discrete-time models are derived. Analytical stability boundaries are found to be consistent with the experimental results. Also the approximate models in [31], [32] would be the special case using the proposed models under the assumption $R/(R + r_c) \approx 1$, where $R$ and $r_c$ are shown in Fig. 1). Further, the proposed small-signal model closely resembles that using accurate models in [30], and the current-loop transfer function correctly matches with that using the well-known Ridley model in [33] and SIMPLIS simulation.

This paper is organized as follows. Section II derives approximate discrete-time models of a synchronous buck converter under MCMC. Fast-scale stability analysis along with the methods for enhanced stability boundary are presented in Section III. Section IV presents discrete-time small-signal modeling and digital controller design. Section V demonstrates experimental results of a buck converter and verifies analytical predictions. Section VI concludes the paper.

**II. DISCRETE-TIME MODELING**

A synchronous buck converter operates under continuous-conduction-mode (CCM), which can take two feasible switch configurations namely Mode 1 when the high-side switch is ON and the Mode 2, otherwise. Referring to the buck converter schematic in Fig. 1, state-space models of these two modes can be derived as follows

$$\dot{x} = A_0 x + (A_1 x + B u) u + A_1 x (1 - u), \quad v_o = C_0 x,$$

(2)

where $x = \begin{bmatrix} i_L & v_{cap} \end{bmatrix}^T$, $i_L$ is the inductor current and $v_{cap}$ is the voltage across the capacitor, and

$$A_0 = \begin{bmatrix} 0 & 0 \\ 0 & -R_n/RC \end{bmatrix}; B = \begin{bmatrix} 1/L \\ 0 \end{bmatrix};$$

$$A_1 = \begin{bmatrix} -R_n r_c/L & -R_n/L \\ R_n/C & -R_n/RC \end{bmatrix};$$

$$C_0 = \begin{bmatrix} R_n r_c & R_n \\ R_n & R \end{bmatrix};$$

where $R = R/(R + r_c)$,

$$v_o (t) = \frac{R r_c}{(R + r_c)} \times i_L (t) + \frac{R}{(R + r_c)} \times v_{cap} (t).$$

(3)
The inductor current \( i_L \) can be assumed to vary linearly with the time; thus \( v_{\text{cap}} \) varies quadratically, which can be written as

\[
i_L(t) = i_{\text{int}} + m_k t,
\]
\[
v_{\text{cap}}(t) = v_{c,\text{int}} + \left(\frac{i_{\text{int}} - i_0}{C}\right) t + \frac{m_k t^2}{2C}.
\]

(4)

where \( i_{\text{int}} \) and \( v_{c,\text{int}} \) are the initial values of \( i_L \) and \( v_{\text{cap}} \), respectively; \( i_0 \) indicates the load current. The slope of the inductor current, \( m_k \), can be written as

\[
m_k = \begin{cases} 1 = \frac{(v_{\text{in}} - v_o)}{L} & \text{during Mode 1} \\ -2 = \frac{v_o}{L} & \text{during Mode 2} \end{cases}
\]

(5)

where \( m_1 \) and \( m_2 \) indicate rising and falling slopes of \( i_L \).

\[
v_\text{e} \quad / \quad v_\text{e}[n] \quad / \quad v_\text{e}[n+1]
\]

\[
i_1 \quad / \quad m_j \quad \text{m} \quad \text{m}_2 \quad / \quad i_{n+1}
\]

\[
(n+1)T \quad / \quad nT \quad d_{\text{n}} T
\]

Figure 3 shows the control waveforms under peak current mode control: Dotted and solid line traces indicate respective waveforms using analog CMC and MCMC schemes with the respective duty ratios \( d_c \) and \( d_n \).

\[
\text{Fig. 3. Control waveforms under peak current mode control: Dotted and solid line traces indicate respective waveforms using analog CMC and MCMC schemes with the respective duty ratios } d_c \text{ and } d_n.\]

The local stability of a system that consists of a set of linear difference equations can be analyzed using the Jacobian matrix \( J_n \) which can be computed as follows

\[
J_n = \frac{\partial x_{n+1}}{\partial x_n} \bigg| x_n = x_n^* = \begin{bmatrix} \frac{\partial i_{n+1}}{\partial i_n} & \frac{\partial i_{n+1}}{\partial v_n} \\ \frac{\partial v_{n+1}}{\partial i_n} & \frac{\partial v_{n+1}}{\partial v_n} \end{bmatrix}.
\]

(14)

The discrete-time current dynamics of a buck converter under continuous conduction mode (CCM) with trailing-edge modulation can be derived using (6)-(8) as

\[
i_{n+1} = i_n + n_1 t_n - m_2 (T - t_n),
\]
\[
v_{n+1} = v_n + m_c \left[ m_1 t_n - \left\{ m_2 (T - t_n) \right\} \right] + \alpha \times
\]
\[
\left[ \left( \frac{i_n - i_0}{C} \right) T - \frac{m_1 t_n^2}{2C} + \frac{m_1 t_n}{C} - \frac{m_2 (T - t_n)^2}{2C} \right].
\]

(9)

1) Discrete-time duty ratio under Mixed-signal CMC

Figure 3 demonstrates the control waveforms of a buck converter under MCMC with trailing-edge modulation. The controller output \( v_c[n] \) represents the peak current reference which remains constant throughout the periodic interval as shown in Fig. 3. The discrete time duty ratio \( d_n \) becomes

\[
d_n = (v_c[n] - i_n) / [(m_1 + m_c) T],
\]

(10)

where \( m_c \) is the slope of the optional compensating ramp \( v_R \) as shown in Fig. 1.

2) Discrete-time duty ratio of analog CMC

The control waveforms under analog CMC are shown using dotted lines in Fig. 3, where the duty ratio \( d_c \) can be derived as

\[
d_c = \frac{v_c(t = d_c T) - i_n}{(m_1 + m_c) T}.
\]

(11)

III. Fast-Scale Stability Analysis and Design Method for Enhanced Stability Boundary

The discrete-time current dynamics of a buck converter under MCMC can be derived using (9) and (10) as

\[
i_{n+1} = \frac{-m_2 t_n}{m_1 + m_c} + \left[ 1 + \frac{m_2}{m_1 + m_c} \right] v_c[n] - m_2 T.
\]

(12)

If the quantized error voltage stays within the zero-error bin (ZEB) [25], i.e., \( v_c[n] = 0 \), the output of the PI controller in (1) becomes constant. Thus the zero-input-stability condition of the current-loop becomes \( m_2 / (m_1 + m_c) < 1 \). In absence of a compensating ramp, i.e., \( m_c = 0 \) in (12), the current-loop of a buck converter, under continuous conduction mode (CCM), will be stable for

\[
|v_{\text{ref}} - (v_c - v_{\text{ref}})| = |D| / (1 - D) < 1 \quad \Rightarrow \quad D < 0.5.
\]

(13)

The stability condition in (13) is quite similar to analog CMC [24]. However, duty perturbations under MCMC for a perturbed initial current may eventually take \( v_c[n] \) outside the ZEB and impose transients in the current-loop. Thus it is necessary to carry out stability analysis of the complete closed-loop system, including the voltage-loop dynamics.

The local stability of a system that consists of a set of nonlinear difference equations can be analyzed using the Jacobian linearization around an operating point [26]. Consider a second-order system with an initial state vector \( x_0 = [i_n, v_n]^T \) which represents the sampled state variables at the beginning of \( n^\text{th} \) clock period. The fast-scale stability of the linearized system can be analytically justified from the eigenvalues of the Jacobian matrix \( J_n \) which can be computed as follows

\[
J_n = \frac{\partial x_{n+1}}{\partial x_n} \bigg| x_n = x_n^* = \begin{bmatrix} \frac{\partial i_{n+1}}{\partial i_n} & \frac{\partial i_{n+1}}{\partial v_n} \\ \frac{\partial v_{n+1}}{\partial i_n} & \frac{\partial v_{n+1}}{\partial v_n} \end{bmatrix}.
\]

(14)
where \( x_e \) is the equilibrium point. This method can be extended for stability analysis under different CMC schemes. Taking partial derivatives of \( i_{n+1} \) and \( v_{n+1} \) in (9), the elements of the Jacobian matrix can be obtained as

\[
\begin{align*}
\frac{\partial i_{n+1}}{\partial i_n} &= 1 + (m_1 + m_2) \frac{\partial i_n}{\partial i_n} \\
\frac{\partial i_{n+1}}{\partial v_n} &= (m_1 + m_2) \frac{\partial i_n}{\partial v_n} \\
\frac{\partial v_{n+1}}{\partial i_n} &= \alpha_r (m_1 + m_2) \frac{\partial i_n}{\partial i_n} + \frac{\alpha T}{C} + \frac{\alpha m_1 T}{C} \frac{\partial i_n}{\partial v_n} - \frac{\alpha T}{C} + \frac{\alpha m_1 T}{C} \frac{\partial v_n}{\partial v_n} \\
\frac{\partial v_{n+1}}{\partial v_n} &= 1 + \alpha_r (m_1 + m_2) \frac{\partial i_n}{\partial v_n} - \frac{1}{R C} \frac{\partial v_n}{\partial v_n},
\end{align*}
\]

where the load current can be taken as \( i_o = v_n/R \).

### A. Fast-scale stability analysis

It is reported in [28], [34] that an integral term will not affect the fast-scale stability boundary. This is because the zero of the PI controller is placed at a low frequency. The integral term is mainly responsible to correct the steady state error, while the fast-scale dynamics is primarily governed by the proportional controller because one of the eigenvalues remains close to unity. Thus the effect of \( k_p \) on fast-scale stability boundary is investigated throughout rest of the paper.

1) **Mixed-signal CMC:** From (1) and (10), it becomes

\[
\frac{\partial t_n}{\partial t_n} = -\frac{1}{(m_1 + \alpha r)}; \quad \frac{\partial t_n}{\partial v_n} = \frac{-k_p}{(m_1 + \alpha r)}.
\]

Using (15) and (16) with \( m_c = 0 \) and with a proportional controller \( (v_c[n] = k_p v_c[n]) \), the Jacobian matrix in (14) can be computed for the MCMC scheme under trailing-edge modulation, and the eigenvalues are found to be

\[
\lambda_{1,2} = \frac{-m_2 - m_1 \delta_2 + k_p m_1 \delta_3 \pm \sqrt{\varphi}}{2m_1},
\]

where \( \varphi = m_2^2 + 2m_1 m_2 \xi_1 + m_1^2 \xi_2 \),
\[
\xi_1 = \delta_2 + k_p (2\delta_1 - \delta_3),
\xi_2 = \delta_2^2 + k_p^2 \delta_3^2 + k_p (4\delta_1 - 2\delta_2 \delta_3),
\delta_1 = -\alpha (m_1 + m_2) r_c/l_1,
\delta_2 = 1 - (\alpha T / RC), \quad \delta_3 = \delta_1 + (\alpha T / C).
\]

From the Eigenvalues, the stability condition becomes

\[
|\lambda| < 1 \Rightarrow k_p < \left( \frac{2RC - T\alpha}{RT} \right) \varepsilon_2
\]

where \( \varepsilon_1 = (m_1 + m_2) \); \( \varepsilon_2 = (m_1 - m_2) \).

The above condition implies an upper limit of \( k_p \) for closed-loop stability of the buck converter. The range depends on the operating voltages, output capacitor, switching time period and the capacitor ESR. Using the parameter set in Sec. I-B, stability boundary is numerically plotted as shown in Fig. 4, in which the input voltage is varied from 6.6 V to 18.6 V and the capacitor ESR is varied from 35 mΩ to 47 mΩ. The above input voltage range with 3.3 V output voltage is selected to highlight fast-scale stability for \( D < 0.5 \), beyond which the current-loop inherently becomes unstable as per (12). The region below the surface in Fig. 4 implies the stable region. This indicates that the stable range of \( k_p \) decreases with the capacitor ESR and increases with the input voltage for \( D < 0.5 \). Figure 3 intuitively shows that because of using uniform sampling, the sampled output voltage is free from ripple due to the output capacitor and its ESR, so as for the controller output. This introduces a delay in MCMC in the switching action compared to analog CMC. This delay increases with increasing ESR and decreasing capacitance, as the voltage ripple increases in either cases; consequently, the stable operating region would be further degraded.

![Fig. 4. Numerical stability boundary of a buck converter under MCMC.](image_url)

### 2) Analog CMC:

It is important to investigate the role of the ESR on the stability of the analog CMC with a proportional controller in the voltage loop and \( m_c = 0 \). With a proportional controller \( G_c(s) = k_p \), the duty ratio expression of (11) can be simplified as

\[
d_c = \frac{v_c[n] - i_n}{\sigma T},
\]

where \( \sigma_1 \) can be derived assuming linear output voltage ripple, primarily dominated by the ESR, which becomes \( \sigma_1 = m_1 + m_1 k_p r_c \). From (21) and (1), it becomes

\[
\begin{align*}
\frac{\partial t_n}{\partial t_n} &= \frac{-1}{(m_1 + m_2)}; \quad \frac{\partial t_n}{\partial v_n} = \frac{-k_p}{(m_1 + m_2)}.
\end{align*}
\]

By following the similar procedure, the Jacobian matrix in (14) can be obtained using (15) and (22); the range of \( k_p \) can be obtained as

\[
|\lambda| < 1 \Rightarrow k_p < \left( \frac{2RC - T\alpha}{\alpha \varepsilon_2 (RT - 2R C r_c) + 2m_1 T \alpha r_c} \right)\varepsilon_2
\]

From (19) and (23), the comparative stability boundary can be obtained as

\[
\frac{k_p,\text{MCMC}}{k_p,\text{CMC}} \approx 1 - \frac{2m_1 r_c (2RC - T\alpha)}{\varepsilon_2 RT + 2R C r_c \alpha},
\]

where \( k_p,\text{MCMC} \) and \( k_p,\text{CMC} \) are the stable gain ranges using MCMC and analog CMC, respectively. For the parameter set considered in Sec. I-B, (24) can be shown to be

\[
0 < k_p,\text{MCMC} < k_p,\text{CMC}.
\]

This indicates that the controller gain range using MCMC is considerably restricted compared to analog CMC; however, a higher \( k_p \) would be needed to achieve fast transient recovery.
Thus it is interesting to investigate whether a ramp compensation can help to enhance the stability boundary.

B. Stabilization via ramp compensation

It is apparent from Fig. 3 that an additional ramp compensation in MCMC can emulate the switching instant close to analog CMC. For a suitable choice of the slope \( m_c \), the switching points using both the techniques can be matched with a reasonable accuracy. This is not possible for a practical converter as the exact parasitic and ripple parameter are not known; however, this can enhance the stability boundary, even for \( D > 0.5 \) [18].

Using (16) and (15), the Jacobian matrix in (14) can be computed for the MCMC scheme along with a ramp compensation. From the eigenvalues of (14), the range of \( k_p \), for a stable operation can be derived as

\[
 k_p < \frac{(2RC - T\alpha)\varepsilon_2}{R\alpha[T\varepsilon_2 + 2Cr\varepsilon_1]} + \frac{2m_c(2RC - T\alpha)}{R\alpha[T\varepsilon_2 + 2Cr\varepsilon_1]}.
\]  

(26)

Thus the range of \( k_p \) can be enlarged by \( \frac{[2m_c(2RC - T\alpha)]}{[R\alpha(T\varepsilon_2 + 2Cr\varepsilon_1)]} \) compared to the uncompensated MCMC scheme given in (19).

C. Stability analysis under leading-edge modulation

Figure 5 demonstrates the control waveforms of a buck converter under MCMC with leading-edge modulation. The error voltage \( v_e[n] \) is sampled at every rising edge of the switching clock \( T_s \), when the high-side MOSFET in Fig. 1 turns off. The switch turns on when the inductor current \( i_L \leq i_c[n] \), where \( i_c[n] \) is the valley current reference that remains constant over the periodic interval. Then the switch continues to remain on throughout rest of the periodic interval. The discrete-time model under the leading-edge modulation can be obtained by following the procedure in Sec. II, considering the sequence of operation starting with the Mode 2 followed by the Mode 1.

The notations of the initial and final values of \( i_L \) and \( v_c \) under trailing-edge modulation are still applicable here, and the duty ratio \( d_n \) can be derived as

\[
d_n = \frac{-i_n + v_c[n]}{(m_2 + m_c)T}.
\]  

(27)

Similar to current dynamics in (28) under trailing-edge modulation, the current dynamics under leading-edge modulation can be derived referring to Fig. 5 and using (27) as

\[
i_{n+1} = \frac{-m_1i_n}{m_2 + m_c} + \left(1 + \frac{m_1}{m_2 + m_c}\right)v_c[n] + m_1T.
\]  

(28)

In absence of a ramp compensation, i.e., \( m_c = 0 \), the zero-input stability condition of the current-loop becomes \( v_{ref} > v_{in}/2 \) which implies that \( D > 0.5 \). Thus the current-loop under leading-edge modulation becomes inherently unstable with the steady-state duty ratio \( D < 0.5 \); consequently, a ramp compensation becomes essential for stabilization. This stability condition is exactly opposite to that using trailing-edge modulation. Thus it is interesting to investigate the impact of the output voltage ripple on the closed-loop stability under uniform sampled leading-edge modulation for \( D < 0.5 \).

1) Effects of the output capacitor and its ESR: Applying partial derivative of (27), it can be written as

\[
\frac{\partial t_n}{\partial v_n} = \frac{-1}{(m_2 + m_c)}; \quad \frac{\partial t_n}{\partial v_m} = \frac{-k_p}{(m_2 + m_c)}.
\]  

(29)

Using (15) and (29) with \( m_c = 0 \), the Jacobian matrix of (14) can be computed for MCMC under leading-edge modulation, and from the eigenvalues, the range of \( k_p \) can be found as

\[
|\lambda| < 1 \Rightarrow k_p < \frac{(2RC - T\alpha)\varepsilon_2}{R\alpha[T\varepsilon_2 + 2Cr\varepsilon_1]}.
\]  

(30)

This shows that the stable-gain range under the leading-edge modulation scheme is similar to that in (19) under trailing-edge modulation; however, in the range of interest for the former, \( \varepsilon_2 < 0 \) with \( D < 0.5 \).

2) Enhanced stability boundary using ramp compensation:

Similar to the trailing-edge modulation, the gain range in (30) can be further extended using an additional compensating ramp. Following the similar methodology, the Jacobian matrix in (14) can be obtained under leading-edge modulation using (15) and (29). From the eigenvalues, the range of \( k_p \) for a stable operation can be derived as

\[
k_p < \frac{(2RC - T\alpha)2m_c}{R\alpha[T\varepsilon_2 + 2Cr\varepsilon_1]} + \frac{(2RC - T\alpha)(-\varepsilon_2)}{R\alpha[T\varepsilon_2 + 2Cr\varepsilon_1]}.
\]  

(31)

Thus a ramp compensation under leading edge can enlarge the range of \( k_p \) by \( \frac{[2m_c(2RC - T\alpha)]}{[R\alpha(T\varepsilon_2 + 2Cr\varepsilon_1)]} \) compared to the uncompensated MCMC scheme given in (30).

A compensating ramp which enlarges the stability boundary can be easily realized using a digital controller; however, its impact on the closed-loop bandwidth should be investigated.

IV. DISCRETE-TIME SMALL-SIGNAL MODELING AND DIGITAL CONTROLLER DESIGN

A. Discrete-Time Small-signal Modeling

Approximate discrete-time models in Sec II are used to analytically derive fast-scale stability condition in (19) for a buck converter under MCMC. It is also important to derive discrete-time small-signal transfer functions. Applying small perturbations followed by linearization, perturbed discrete-
The current-loop in MCMC is in the analog domain; thus the closed current-loop needs to be justified. Taking partial derivative of (10) with \( m_c = 0 \), it becomes
\[
\partial d_n = \frac{1}{M_1 T} \left[ \partial v_c[n] - \partial i_n \right] - \frac{D_n T \partial v_{in}}{M_1 L T} \tag{34}
\]
Substituting (34) in (33), the Jacobian matrix is obtained as
\[
\begin{bmatrix}
\partial i_{n+1} \\
\partial v_{n+1}
\end{bmatrix} =
\begin{bmatrix}
a_{11} & a_{12} \\
a_{21} & a_{22}
\end{bmatrix}
\begin{bmatrix}
\partial i_n \\
\partial v_n
\end{bmatrix} +
\begin{bmatrix}
b_1 \\
b_2
\end{bmatrix} \partial d_n +
\begin{bmatrix}
e_1 \\
e_2
\end{bmatrix} \partial v_{in},
\tag{35}
\]
where
\[
a_{11} = 1, \ a_{12} = \frac{\alpha T}{L}, \ a_{21} = 0, \ a_{22} = 1 - \left( \frac{\alpha T}{L} \right) - \frac{\alpha D_n r_c T}{L}, \ b_1 = T \left( M_1 + M_2 \right), \ b_2 = \alpha r_c T \left( M_1 + M_2 \right) / (r_c C), \ e_1 = 0 \text{ and } e_2 = \frac{-\alpha D_n r_c T}{L}.
\]
Thus the control-to-output transfer function can be obtained using duty ratio as the control input, as
\[
G_{oc}(z) = \frac{z b_2 + b_1 a_{21} - a_{11} a_{22}}{z^2 - z \left( a_{11} + a_{22} \right) - a_{12} a_{21} + a_{11} a_{22}}.
\tag{36}
\]
A comparative study of current-loop control-to-output transfer functions using various methods are shown in Fig. 7 using the parameter set in Sec. I-B. This shows that the proposed model closely resembles that using the Ridley model in [33] and that obtained using SIMPLIS simulation.

The discrete-time models derived in Sec. II are accurate enough to predict fast-scale instability as well as to capture small-signal behavior. Thus the transfer function in (36) can be used to design the controller \( G_c(z) \) directly in digital domain.

### B. Effect of ramp compensation on the closed loop bandwidth

It is well known that a compensating ramp with a higher slope tends to degrade the closed-loop bandwidth of a CMC buck converter [33], which is equally applicable for MCMC as shown in Fig. 8. The closed-loop transfer function is obtained using the proposed discrete-time model. The Bode plots demonstrate that a higher value of \( m_c \) reduces the gain at high frequency; however, the closed-loop bandwidth degrades, thereby slowing down the transient response. Thus, it is important to select a suitable ramp slope using (26), which would stabilize the closed-loop converter.

An alternative approach is to select a dynamic ramp compensation, in which \( m_c \) is disabled during a large-signal transient and enabled when the output voltage reaches close to the desired voltage. This reconfigurable slope compensation can be easily carried out in digital domain, which would improve the dynamic performance without comprising the stability. This requires to detect transients and steady-state conditions, which provide design and implementation opportunities.

### C. Static quantization requirements

Dynamic stability conditions which are derived in Sec. III are the necessary stability conditions under MCMC. However,
those are not sufficient to guarantee a stable periodic operation, neither enough to meet the regulatory requirement, because of the finite word-length effect. Although the analog current-loop in MCMC can achieve an infinite duty ratio resolution; the finite word-length of the digital voltage controller as well as the A/D converter would impose an overall duty ratio resolution. Thus it is important to meet quantization requirements to keep the quantized error \( Q(v_c[n]) \) inside the ZEB, and the design guidelines are presented in [17]. Also the discrete-time integral gain should satisfy that \( 0 < k_i < 1 \), in order to avoid any steady-state limit cycle oscillation [25].

D. Staircase effects due to discrete-time ramp compensation

Figure 9 shows the control waveforms of MCMC, where both the continuous-time and discrete-time compensating ramps are considered. Thus \( i_L \) intersects the reference current at different time instants when their discrete-time equations become

\[
\begin{align*}
  v_c[n] &= i_n + m_1 d_c T + m_c d_c T, \\
  v_c[n] &= i_n + m_1 d_n T + m_c t_{\text{clk}} \times \text{floor}(d_c T/t_{\text{clk}}),
\end{align*}
\]

(37)

where \( q \) and \( t_{\text{clk}} \) are the DPWM voltage resolution and the time period of the DPWM clock. Thus the duty ratio error \( d_c \) using both the compensating ramps can be derived as

\[
d_c = d_n - d_c = \frac{q \times \text{frac}(x)}{(m_1 + m_c) T}, \quad x = \frac{m_c d_c T}{q} = \frac{d_n T}{t_{\text{clk}}}, \quad (38)
\]

where \( \text{frac}(x) \) indicates the fractional part of a real number \( x \), which can be written as \( \text{frac}(x) = x - \text{floor}(x) \). This non-zero \( d_c \) in (38) will not allow the current-loop to completely settle down to a steady-state solution. While an analog CMC technique can be stabilized through a suitable choice of \( m_c \) in (12), the same stability condition is not readily applicable to completely stabilize the MCMC scheme. It is clear from (38) that the discrete-time ramp should have enough resolution to avoid sub-harmonic instability. The quantization analysis for the MCMC technique is presented in [17], and the analysis shows that the overall resolution is also linked with the bit-size of the D/A converter. For an \( N \) bit DAC, the required clock period \( t_{\text{clk}} \) can be calculated using [17] as

\[
t_{\text{clk}} = \frac{v_r}{2^N \times m_e}, \quad (39)
\]

where \( v_r \) is the reference voltage of the DAC.

E. Summarized design steps

The overall design steps are summarized below:

**Step I:** Based on the parameter set and operating conditions, design the PI controller in (1) using the discrete-time small-signal transfer function in (36) directly in the digital domain using a transformed domain approach [19]. MATLAB SISO tool box can be used for off-line design for different operating points, and a loop-up-table (LUT)-based approach may be used to store the controller parameters and the operating points.

**Step II:** The discrete-time integral gain \( k_i \) in (1) must satisfy \( 0 < k_i < 1 \). This is the necessary condition to avoid limit cycle oscillations [25] by keeping \( v_r[n] \) within the ADC’s ZEB, when the integrator DC component is the controller output.

**Step III:** After obtaining \( k_p \), select a suitable ramp slope \( m_c \) using (26) to ensure fast-scale stability of the buck converter using the MCMC technique.

**Step IV:** Using the computed value of \( m_c \), verify the closed-loop bandwidth. If it meets the specified bandwidth, then ramp compensation can be used throughout. Otherwise, a transient detection circuit is needed to use a reconfigurable \( m_c \), which is disabled during a transient and enabled during steady-state.

**Step V:** Finally, the ramp resolution should satisfy (39) to overcome the staircase effect of the discrete-time ramp.

V. HARDWARE IMPLEMENTATION

A buck converter prototype has been made, and the MCMC scheme is implemented using a Virtex-5 FPGA kit. A nominal set of power circuit components in Sec. I is considered here and a discrete-time integral gain \( k_i = 0.055 \) is considered for all the test results. For the prototype signal conditioning circuits, a 10-bit differential pipeline ADC (AD9215) is considered to sample the output voltage. This uses a differential amplifier (AD8138) to convert the single-ended output voltage into the differential form for reduction in common mode noise. The digital output of the voltage-loop compensator \( G_c(z) \) is converted into an analog voltage \( v_A \) using a 12-bit DAC (AD9762) followed by a differential receiver amplifier (AD8130). The output is then directly compared with the sensed inductor current in the analog domain using a high speed analog comparator (TLV3501). For inductor current sensing, a 10 m\( \Omega \) shunt is used and the differential voltage
is converter into an equivalent single-ended voltage using a fixed-gain (high-side) current sense amplifier (ADM4073). The switching frequency is taken to be 200 kHz for the MCMC scheme in Fig. 1.

A. Steady-state stability status

1) Mixed-signal CMC under trailing-edge modulation: Figure 10 shows the stability status of a synchronous buck converter governed by the MCMC scheme under trailing-edge modulation. For a smaller proportional gain with \( k_p = 0.75 \), Fig. 10(a) shows that the buck converter remains stable, and the FFT trace renders the fundamental and harmonic contents for the nominal switching of 200 kHz. However, for a higher proportional gain with \( k_p = 5 \), Fig. 10(b) clearly shows sub-harmonic instability. This is also evident from the FFT trace which shows spectral peaks at 100 kHz (sub-harmonic component). Now considering a ramp compensation for a suitable choice of \( m_c \) using (26), the upper limit of \( k_p \) can be increased and the closed-loop buck converter can be stabilized as shown in Fig. 10(c). Thus a ramp compensation restores a stable periodic operation at higher controller gain, and the FFT trace shows sharp peaks at fundamental and harmonic contents. Further, all the above experimental results are more or less consistent with the simulation results and also with the analytical predictions.

2) Mixed-signal CMC under leading-edge modulation: Figure 11 shows the stability status under the MCMC scheme with leading-edge modulation. For a smaller proportional gain with \( k_p = 0.75 \), Fig. 11(a) shows that the buck converter remains stable, and the FFT trace renders the fundamental and harmonic contents for the nominal switching of 200 kHz. However, for a higher proportional gain with \( k_p = 5 \), Fig. 11(b) clearly shows sub-harmonic instability, and the FFT trace shows spectral peaks at 100 kHz (sub-harmonic component). Incorporating a ramp compensation with a suitable choice of \( m_c \) using (31), the upper limit of \( k_p \) can be increased and the closed-loop buck converter can be stabilized as shown in Fig. 11(c). This restores a stable periodic operation using a ramp compensation. Moreover, the experimental results are found to be more or less consistent with the simulation results and also with the analytical predictions.

B. Staircase effects of discrete-time ramp compensation

A higher DPWM controller clock can achieve a high resolution discrete-time ramp which would attempt to lock the error voltage inside the ZEB. Thereafter, a stable periodic operation can be achieved by satisfying dynamic stability conditions. For a poor ramp resolution using a lower frequency DPWM clock, the error voltage cannot be kept inside the ZEB. This results in sub-harmonic instability as shown in Fig. 12, and the FFT trace shows spectral peaks at 100 kHz (sub-harmonic component). Using a longer time period with \( t_{clk} = 300 \) ns; thus the duty ratio error in (38) increases. Thus it is important to suitably select the ramp resolution to achieve a stable operation.
C. Load transient performance

Figures 13–15 show the transient performance of a synchronous buck converter using the MCMC scheme for a step change in load current from 3 A to 9 A at 8 V input under different proportional gains. Figure 13 shows that a lower $k_p$ can achieve a stable periodic operation. However, this results in the slower transient performance with 0.48 ms settling time and 400 mV voltage undershoot. A higher proportional gain significantly improves the transient performance with 0.28 ms settling time and 200 mV voltage undershoot; however, this results in sub-harmonic instability which is shown in Fig. 14. The closed-loop converter with a higher $k_p$ can be stabilized by incorporating a ramp compensation as shown in Fig. 15. All the test results in Figs. 10–15 demonstrate that the desired steady-state regulation can be achieved under stable periodic behavior and keeping $v_e$ inside the ADC’s ZEB.

Analytical stability boundaries and discrete-time small-signal models in this paper are helpful to design stable digital current-mode control with fast transient performance in a CCM buck converter. Under light load conditions, the low-side MOSFET in Fig. 1 is turned off to operate the converter under discontinuous conduction mode (DCM) when the body diode conducts. While operating in DCM, it was found that, unlike in CCM, the closed-loop stability does not get considerably affected by the voltage ripple. Also test results under digital VMC were found to be stable in [35].

VI. Conclusion

This paper proposed a unified discrete-time framework to (i) formulate closed-form stability conditions, (ii) identify methods for enhanced stability boundary, and (iii) derive discrete-time small-signal transfer functions for direct digital controller design to meet the desired specifications. Stability analysis demonstrated that the use uniform output voltage sampling would significantly restrict the stable range of the controller gain, and a compensating ramp would enhance the stability boundary. A buck converter prototype was tested, and
the analytical predictions were verified experimentally. The proposed framework would be useful for the designers to devise a stable mixed-signal current mode controller over a wide operating range along with improved transient performance.

REFERENCES


