Abstract—The output voltage of a voltage-mode digitally pulse-width-modulated (DPWM) DC-DC converter is sampled once per switching cycle, and past studies show the existence of limit cycle oscillations due to quantization. This brief reports that the map of a continuous conduction mode (CCM) buck converter under DPWM is shown to be discontinuous and exhibits border collision bifurcations mainly because of a sampling delay. The discrete-time state space is piecewise smooth, divided into nine regions with different functional forms and separated by eight boundaries. This is unlikely using analog PWM, in which only three regions and two borders exist under CCM. The closed-form stability conditions are derived and design methods are discussed to enhance the stability boundary. A prototype buck converter is tested. Experimental bifurcation diagrams and time domain results are demonstrated to support the analytical predictions.

Index Terms—Voltage-mode, digital control, DPWM, sampling delay, non-smooth bifurcations, synchronous buck converter.

I. INTRODUCTION

Voltage-mode DPWM in DC-DC converters is useful for portable devices [1]. Past studies reported the existence of limit cycle oscillations due to finite quantization [2], even more complex nonlinear phenomena in [3], [4]. Nonlinear phenomena were extensively studied in DC-DC converters using voltage-mode control (VMC) [5]–[8], including smooth and non-smooth bifurcations. Border collision bifurcations were reported in VMC DC-DC converters [7]–[11], in which only three regions and two borders exist under CCM [9], [10].

However, to the best of my knowledge, such investigations have not been reported so far by considering finite sampling and quantization effects in the context of a DPWM converter. The objective of brief is to investigate the effect due to finite sampling in a DPWM converter, which may lead to more severe border collision bifurcations compared to an analog PWM.

This brief is organized as follows. Section II discusses a DPWM synchronous buck converter and possible switch configurations. Section III develops exact discrete-time models. Section IV presents bifurcation analysis and design methods using experimental case studies. Section V concludes the brief.

II. VOLTAGE-MODE DPWM IN A BUCK CONVERTER

Fig. 1 shows the schematic of a DPWM voltage-mode controlled (DVMC) synchronous buck converter. A DPWM block is realized using a counter that gets incremented using the main clock $F_{\text{clk}}$ and is reset when its output $v_{\text{up}}$ reaches an upper limit $v_{\text{up}}$. The comparator output is used as the switching frequency clock $F_{\text{sw}}$. The key control waveforms of a practical DVMC converter are shown in Fig. 2. An ADC is used to sample the output voltage $v_n$ using the sampling clock $F_{\text{sv}}$, and the zero-order-hold effect maintains the sampled voltage $v_n[n]$ till the arrival of the next rising edge of $F_{\text{sv}}$. The edge of $F_{\text{sv}}$ must appear well before that of $F_{\text{sw}}$ in order to capture clean $v_n$ and to provide sufficient time for ADC conversion and (digital) controller computation; thus a (lumped) sampling-delay $t_s$ is considered as shown in Fig. 2.

Using the sampled voltage $v_n[n]$ and the reference voltage $v_{\text{ref}}$, an error voltage $v_{\text{err}}[n]$ is generated. The digital voltage controller $G_C$ computes using the same rate of $F_{\text{sv}}$, and its output $v_{\text{eq}}[n]$ is compared with the ramp signal $r_{\text{th}}$ which is the output of the DPWM block as shown in Fig. 1. The comparator output is directly used as the gate signal $u$ as $v_{\text{eq}}[n]$ is updated once per switching cycle. Using $u$, a half-bridge gate driver (UCC27211) generates the respective high-side and low-side gate signals $u_{\text{H}}$ and $u_{\text{L}}$ of the N-channel MOSFETs (FDS6699) with a finite dead-time in between.
A. Details of hardware implementation

A Virtex-5 FPGA kit is used as the digital implementation platform in Fig. 1. A buck converter prototype is made with the respective \( F_{\text{clk}} \) and \( F_{\text{sw}} \) clocks taken as 100 MHz and 200 kHz. A 9-bit DPWM counter is considered. A pipeline ADC (AD9215) is used to sample \( v_o \). A nominal parameter set is considered below for all the numerical and experimental test cases: \( L = 10 \mu \text{H}, C = 470 \mu \text{F}, v_{\text{in}} \in [5, 15] \text{ V}, v_{\text{ref}} = 3.3 \text{ V}, R = 1.4 \Omega, r_c = r_{eq} = 20 \text{ m\Omega}, \) and \( t_s = 0.8 \mu \text{s} \) for the nominal switching frequency of 200 kHz, i.e., \( T = 5 \mu \text{s} \).

B. Possible switch configurations within a periodic cycle

In Fig. 2, \( M_1 \) indicates the mode when \( u = 1 \), the high-side MOSFET in Fig. 1 remains ON, and the inductor current \( i_L \) ramps up; \( M_2 \) is the mode when \( u = 0 \), the high-side MOSFET remains OFF, and \( i_L \) decreases. During the \( n \)th sampling interval, the desired periodic sequence consists of \( M_2 \rightarrow M_1 \rightarrow M_2 \), and its operation is referred to be in the region R1. For the same sampling interval, there exist eight other possible, though undesirable, periodic sequences which along with their respective regions are shown in Fig. 3.

III. DISCONTINUOUS DISCRETE-TIME STATE SPACE

A. State-space equations and their solutions

Referring to Fig. 1, the state variables are taken as \( x_1 = i_L \) and \( x_2 = v_c \), and the state-space model can be written as
\[
\dot{x} = Ax + uBv_{\text{in}}; \quad v_o(t) = C_m x(t); \quad x = [x_1, x_2]^T,
\]
where \( u = 1 \) for mode \( M_1 \) and \( u = 0 \) for mode \( M_2 \), and
\[
A = \begin{bmatrix}
-\frac{r_c}{C} & -\frac{1}{RC} \\
\frac{1}{C} & -\frac{R}{RC}
\end{bmatrix}, \quad B = \begin{bmatrix}
\frac{1}{C} \\
0
\end{bmatrix}, \quad C_m = \begin{bmatrix}
\alpha r_c & \frac{1}{R}
\end{bmatrix}^T,
\]
where \( r_c = r_{eq} + \alpha r_c \) and \( \alpha = R/(R + r_c) \). The solution of the state-vector in (1) can be written as
\[
x(t) = e^{A(t-t_0)} x_0 + \left\{ I - e^{-A(t-t_0)} \right\} A^{-1} u B v_{\text{in}}, \quad (2)
\]
where \( t_0 \) and \( x_0 \) are the initial time and state vector, and the system matrix \( A \) is non-singular. The solution in (2) can be used for mode \( M_1 \) using \( u = 1 \) and mode \( M_2 \) using \( u = 0 \).

B. Discrete-time models for different periodic configurations

Let the state vector in (2) at the beginning of the \( n \)th sampling interval be \( x_n \) and that of the end of the interval be \( x_{n+1} \). Discrete-time models related to nine different regions, as discussed in Sec. II-B, can be derived, using (2), considering their respective sequences of modes along with their durations.

1) Region R1: Fig. 2 shows a periodic sequence of \( \{M_2 \rightarrow M_1 \rightarrow M_2\} \) with the respective durations of \( t_s, d_n T, \) and \( (T - d_n T - t_s) \); thus the complete discrete-time map becomes
\[
x_{n+1} = e^{AT} x_n + \left[e^{A(T-t_s)} - e^{A(T-d_n T)}\right] A^{-1} B v_{\text{in}}. \quad (3)
\]

2) Region R2: Fig. 3 (a) shows a periodic sequence of \( \{M_2 \rightarrow M_1\} \) with the respective durations of \( t_s \) and \( (T - t_s) \); thus the complete discrete-time map can be derived as
\[
x_{n+1} = e^{AT} x_n + \left[e^{A(T-t_s)} - I\right] A^{-1} B v_{\text{in}}. \quad (4)
\]

3) Region R3: Fig. 3 (b) shows that only the mode \( M_2 \) operates throughout the sampling (periodic) interval \( T \); thus the complete discrete-time map can be derived as
\[
x_{n+1} = e^{AT} x_n. \quad (5)
\]

4) Region R4: Fig. 3 (c) shows a periodic sequence of \( \{M_1 \rightarrow M_2\} \) with the respective durations of \( (d_n T + t_s) \) and \( (T - d_n T - t_s) \); thus the complete discrete-time map becomes
\[
x_{n+1} = e^{AT} \left[x_n + \left(I - e^{-A(d_n T + t_s)}\right) A^{-1} B v_{\text{in}}\right]. \quad (6)
\]

5) Region R5: Fig. 3 (d) shows that only the mode \( M_1 \) operates throughout the sampling (periodic) interval \( T \); thus the complete discrete-time map can be derived as
\[
x_{n+1} = e^{AT} x_n + \left(e^{AT} - I\right) A^{-1} B v_{\text{in}}. \quad (7)
\]

6) Region R6: Fig. 3 (e) shows a periodic sequence of \( \{M_1 \rightarrow M_2\} \) with the respective durations of \( t_s \) and \( (T - t_s) \); thus the complete discrete-time map can be derived as
\[
x_{n+1} = e^{AT} \left[x_n + \left(I - e^{-A t_s}\right) A^{-1} B v_{\text{in}}\right]. \quad (8)
\]

7) Region R7: Fig. 3 (f) shows a periodic sequence of \( \{M_1 \rightarrow M_2 \rightarrow M_1\} \) with the respective durations of \( (t_s - T + d_{n-1} T), (T - d_{n-1} T), d_n T, \) and \( (T - d_n T - t_s) \); thus the complete discrete-time map can be derived as
\[
x_{n+1} = e^{AT} \left[x_n + A_1 A^{-1} B v_{\text{in}}\right], \quad \text{where} \quad A_1 = I + e^{-A t_s} - e^{A(T - t_s - d_{n-1} T)} - e^{-A t_s} - e^{A(T - d_n T - t_s)}.
\]

8) Region R8: Fig. 3 (g) shows a periodic sequence of \( \{M_1 \rightarrow M_2 \rightarrow M_1\} \) with the respective durations of \( (t_s - T + d_{n-1} T), (T - d_{n-1} T), \) and \( (T - t_s) \); thus the complete discrete-time map can be derived as
\[
x_{n+1} = e^{AT} x_n + A_2 A^{-1} B v_{\text{in}}, \quad \text{where} \quad A_2 = e^{AT} + e^{A(T-t_s)} - e^{A(2T-t_s - d_{n-1} T)} - I.
\]

9) Region R9: Fig. 3 (h) shows a periodic sequence of \( \{M_1 \rightarrow M_2\} \) with the respective durations of \( (t_s - T + d_{n-1} T) \) and \( (2T - t_s - d_{n-1} T) \); thus the complete discrete-time map can be derived as
\[
x_{n+1} = e^{AT} \left[x_n + \left(I - e^{-A(T-t_s - d_{n-1} T)}\right) A^{-1} B v_{\text{in}}\right]. \quad (11)
\]

The discrete-time maps in (3) – (11) are discontinuous, which must be separated by borderlines as discussed below.

C. Derivation of border conditions

Let \( v_{n-1} \) and \( v_n \) be the respective sampled output voltages during \((n-1)\)th and \(n\)th sampling intervals, which are needed along with the parameters of the digital voltage controller \( G_c \) (in Fig. 1) to derive the borderlines. Considering \( G_c \) as a discrete-time proportional-integral (PI) controller, its output
during the $n^{th}$ sampling interval, $v_{co}[n]$ can be written as

$$v_{co}[n] = k_p (v_{ref} - v_n) + u_1[n];$$

$$u_1[n] = u_1[n-1] + k_1 (v_{ref} - v_n) ,$$

where $k_p$ and $k_1$ are the proportional and discrete-time integral gains.  

1) **Border $v_{b2}$**: From Figs 3 (c) and (f), there exists a border condition at the $n^{th}$ rising edge of $F_{vs}$, which separates the regions R4 and R7. Considering a proportional controller, i.e., $u_1 = 0$ in (12), the border condition $v_{b2}$ can be found as

$$k_p (v_{ref} - v_{b1}) = m_e T \Rightarrow v_{b1} = v_{ref} - (m_e T/k_p),$$

where $m_e$ is the slope of the ramp signal $v_t$ in Fig. 1.

2) **Border $v_{b3}$**: From Figs 2 and 3 (a), there exists a border condition at the $(n+1)^{th}$ rising edge of $F_{vs}$, which separates the regions R1 and R2. With setting the term $u_1 = 0$ in (12), the border condition $v_{b3}$ can be found as

$$k_p (v_{ref} - v_{b2}) = m_e (T - t_s) \Rightarrow v_{b3} = v_{b1} + m_e T/k_p.$$  

3) **Border $v_{b3}$**: From Figs 2 and 3 (b), there exists a border condition which separates the regions R1 and R3. With the term $u_1 = 0$ in (12), the border condition $v_{b3}$ can be found as

$$k_p (v_{ref} - v_{b3}) = 0 \Rightarrow v_{b3} = v_{ref}.$$ 

**D. Discrete-time parameter-space**

The complete discrete-time parameter-space of a CCM buck converter under voltage-mode DPWM with proportional control is shown in Fig. 4. The figure represents a two-dimensional (2-D) parameter-space with nine regions R1 to R9, related to nine configurations in Figs 2 and 3. These are separated by eight boundaries that are formed by the initial conditions $v_{n-1}$, $v_n$, and the borderlines $v_{b1}$ to $v_{b3}$. It is important to observe from (13) and (14) that the region R1 which links with the desired period-1 orbit, shrinks with increasing $k_p$ and $t_s$. For a given $t_s$, the region R1 can be enlarged by increasing the ramp slope $m_e$ and/or decreasing $k_p$, and these facts are consistent with the practices using analog PWM [10]. However, either of these methods tends to degrade the closed-loop bandwidth.

If the sampling-delay $t_s = 0$ in case of analog PWM, $v_{b2} = v_{b1}$, and $v_{n-1}$ axis in Fig. 4 does not exist. This results in 1-D parameter-space with three regions in a periodic cycle with (i) $u = 0$, (ii) $u = 1$, or (iii) $u$ changes its state from logic 1 to 0 in between, and the regions are separated by $v_{b1}$ and $v_{b3}$.

**IV. BIFURCATION ANALYSIS AND ENHANCED STABILITY**

**A. Numerical bifurcation diagram and stability analysis**

![Bifurcation diagram](image)

Without considering quantization, Fig. 5 shows that at $v_{in} = 8$ V, a period-1 orbit losses stability and gives rise to a period-2 orbit with a discrete jump. However, it requires an in-depth analysis to understand the way a period-1 orbit losses stability. A first-order approximation is used for $e^AT$, and second-order approximations are used for $e^{A(T-t_s)}$ and $e^{A(T-t_s-d_t)T}$ to retain $t_s$; thus the perturbed dynamics of (3) can be written as

$$\dot{x}_{n+1} = [I + AT] \dot{x}_n + \left[I + A\{(1 - D) T - t_s\}\right] Bv_{in} T \ddot{d}_n,$$

where $D$ is the steady-state duty ratio. Using (12), the perturbed duty ratio $\ddot{d}_n = -k_p v_{in}/m_e$, which is substituted in (3) and (16) to obtain the perturbed closed-loop dynamics. Under the same condition as in Fig. 5, the locus in Fig. 6 shows that the discrete-time eigenvalues are initially complex conjugate, which become real and move along with the real axis for increasing $v_{in}$. One eigenvalue goes out of the unit
circle from the left-side of the real-axis at $v_{in} \geq 8.3$ V; thus the period-1 orbit becomes unstable through a smooth bifurcation. The critical analytical value of $v_{in}$ deviates a little bit from its numerical value in Fig. 5 at $v_{in} = 8$ V, which is because of using lower-order approximations of matrix exponentials.

A closer look near $v_{in} = 8$ V in Fig. 5 reveals that a period-1 orbit loses stability via a period doubling which occurs for a narrow range, $v_{in} \in [7.99, 7.999]$ V, and the nature of smooth bifurcation is consistent with the analysis in Fig. 6. At $v_{in} = 8$ V, the converter initially exhibits smooth period-doubling, and after few subsequent cycles, $v_{n}$ crosses the border $v_{b3}$ in Fig. 4 from the below, the operation moves out of the region R1, and toggles between the regions R2 and R3. In presence of the delay $t_{O}$, $v_{n-1}$ crosses the border $v_{b2}$ from the above, and the combined operation includes the region R7. Here $v_{n-1}$ and $v_{n}$ dynamically change, which results in high periodic orbits along with co-existing attractors with a few narrow ranges of $v_{in}$. Using a higher $k_{p}$, a further increase in $v_{in}$ tends to move the initial conditions to other regions in Fig. 4, thereby leading to high periodic behavior with duty ratio saturations in Fig. 5. Such non-smooth bifurcations may not occur in analog PWM.

$\text{v}_{in}$, beyond 13 V, leads to abrupt high-periodic behavior with duty ratio saturations as evident from Fig. 8 (d) for $v_{in} = 15$ V.

![Fig. 6. Locus of closed-loop eigenvalues in the Z-plane with varying $v_{in}$.](image)

**B. Experimental bifurcation analysis**

For all the test cases, $k_{p} \in [30, 100]$, and an integral gain of $k_{i} = 0.02$ in (12) is considered to meet the quantization requirement [2] using up to 7 MSBs of the ADC for a 9-bit DPWM. Since $k_{i} \ll k_{p}$, the borders can be derived in this case using (13) – (15) and adding $u_{1} \approx m_{c}DT$ with $v_{co}[n]$ in (12). For all the time domain test results, Ch 1, Ch 2, and Ch 3 indicate $v_{in}$, $i_{L}$, and $v_{o}$ (shown in Fig. 1), respectively.

The experimental bifurcation diagram in Fig. 7 shows that, under the same operating condition, the nature of bifurcation behavior closely matches with that in Fig. 5. However, for $v_{in} \leq 6.8$ V, high periodic orbits are found for the test case, which is primarily due to the ADC quantization effect. At $v_{in} = 6$ V, Fig. 8 (a) shows that the operation initially stays in the region R1 when the quantized error voltage, $Q[v_{e}]$ stays within the ADC zero-error-bin (ZEB) [2]; however, the output voltage $v_{o}$ slowly increases. After 10 to 15 consecutive cycles, $Q[v_{e}]$ comes out of the ZEB, which leads to a discrete (negative) jump in the controller output, and $v_{o}$ hits the border $v_{b3}$. Thus the operation jumps to the region R3, and may jump to the region R2, before coming back to the region R1 again.

Fig. 8 (b) shows stable period-1 orbit for $v_{in} \in [6.8, 8.3]$ V. Above 8.3 V input, period-1 orbit losses stability and gives rise to co-existing attractors as shown in Fig. 8 (c). A higher

![Fig. 7. Experimental bifurcation diagram with $k_{p} = 50$ and 7-bit ADC.](image)

**C. Effects due to quantization resolution**

A higher ZEB size, compared to Fig. 8 (a), can be achieved by reducing the ADC resolution to $N_{ad} = 6$ bits in Fig. 9 (a). This allows more flexibility to slowly settle $v_{o}$, which results in a stable period-1 orbit for an extended range $v_{in} \in [5, 10.2]$ V. While a smaller $N_{ad}$ improves stability, it degrades the steady-state voltage regulation [2], and makes it difficult to trade-off.

If the ADC resolution is set to $N_{ad} = 8$ bits for $N_{dpwm} = 9$ bit DPWM resolution, even a small change in $v_{o}$ takes $Q[v_{e}]$ out of the (smaller in size) ZEB. This causes frequent discrete jumps in the controller output, and makes it more susceptible to hit the nearby borders, thereby taking the operation in the multiple regions in the parameter-space (in Fig. 4). Fig. 9 (b) shows the existence of mainly high periodic orbits along with co-existing attractors within a few narrow ranges of $v_{in}$.
Fig. 9. Experimental bifurcation diagrams obtained under the same test conditions in Fig. 7, however, using different ADC resolutions.

Fig. 11. (a) Effects due to finite quantization: Simulated bifurcation diagrams using the ADC resolutions (a) $N_{\text{ad}} = 8$ and (b) $N_{\text{ad}} = 9$ bits.

Fig. 10 (a) shows steady-state waveforms related a co-existing attractor at $v_{\text{in}} = 7.5$ V. For a higher $v_{\text{in}}$, Fig. 10 (b) shows abrupt high-periodic behavior with duty ratio saturations. If the ADC resolution is set to $N_{\text{ad}} = N_{\text{dpwm}} = 9$ bits, the duty resolution becomes insufficient to keep $Q[v_c]$ within the ZEB, because the quantization requirement of $N_{\text{ad}} < N_{\text{dpwm}}$ in [2], is violated. This along with switching noises in the ADC least-significant-bits result in high periodic orbits throughout the entire input voltage range as shown in Fig. 9 (c).

Fig. 11 (a) shows that the staircase effect of the discrete-time ramp $v_R$ (in Fig. 1) results in a finite duty ratio resolution $\Delta d_n = t_{\text{clk}}/T$, where $t_{\text{clk}}$ is the time period of the controller clock. The quantized controller output $Q[v_{\text{co}}]$ imposes an extra constraint on $\Delta d_n$. These require the ADC resolution to satisfy $N_{\text{ad}} < N_{\text{dpwm}}$ to lock $Q[v_c]$ within the ZEB [2]. Numerical bifurcations diagrams in Figs. 11 (b) and (c) are obtained using the models in (3) - (11) for the same operating conditions of the respective experimental diagrams in Figs. 9 (b) and (c). Theoretical analysis seems to be consistent with the experimental results and confirms the existence of mainly high periodic orbits along with co-existing attractors within a few narrow ranges of $v_{\text{in}}$ for $N_{\text{ad}} = 8$ and 9 bits. However, a stable period orbit is achievable for $N_{\text{ad}} \leq 7$ bits with $N_{\text{dpwm}} = 9$, and it is practically recommended to use $N_{\text{ad}} = N_{\text{dpwm}} - 2$ for a better trade-off between the stability and regulation.

D. Stability enhancement using a higher ramp slope $m_c$

As discussed in Section III-D, it is practically possible to enlarge the stable range of the region R1 (period-1 behavior) by increasing $m_c$, even with increasing $k_p$ for $N_{\text{ad}} = 7$. Alternatively, $k_p$ can be reduced to enhance the stability boundary. In fact, stable period-1 orbit is found over the entire range of $v_{\text{in}}$ from 5 to 15 V using $m_c > 2.8$ V/\mu s or using $k_p < 30$. The real-time configuration using the voltage-mode DPWM allows one to use smaller $m_c$ and higher $k_p$ during transients, which need to be accordingly adjusted near steady-state conditions for stable periodic behavior.

V. CONCLUSIONS

In this brief, sampling-induced border collision bifurcations were reported both analytically and experimentally, for the first time, in a digitally voltage-mode controlled buck converter. The proposed analytical framework can be extended to other digital control methods as well as DC-DC converter topologies and is useful to design high-performance stable digital control.

REFERENCES