Selectively Sampled Sub-harmonic Free Digital Current Mode Control Using Direct Duty Control

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Abstract—Benefits of digital current mode control are often limited by the choice of current-loop sampling rate. A higher rate requires a fast analog-to-digital converter which consumes substantial power and increases cost. A lower rate often results in sub-harmonic oscillations, even using a programmable ramp compensation. This paper proposes a simple technique to compute the steady-state oscillations in real-time while the closed-loop controller is in action. A time-to-digital converter translates cycle-by-cycle duty ratio information into digital code, and a ‘duty ratio computation’ block generates the computed duty ratio using an moving average filter. At steady-state, this enforces a virtual open-loop configuration and completely disables current-loop sampling and controller computation, thereby saving substantial power and eliminating sub-harmonic oscillations. Considering a DC-DC buck converter as the test case, it is found that even in presence of high periodic behavior under the closed-loop control, a near-ideal steady-state duty ratio can be reconstructed. Design related issues with duty ratio saturation are discussed with test cases.

Index Terms—Duty ratio computation, digital current mode control, selective sampling, limit cycle, sub-harmonic oscillations.

I. INTRODUCTION

DIGITAL control offers several technical and cost benefits [1]–[10]; however, such benefits are often limited by the choice of current-loop sampling rate in Digital Current Mode Control (DCMC). A higher rate requires a fast analog-to-digital converter which consumes substantial power and increases cost. A lower rate often results in sub-harmonic oscillations. This paper addresses some of these issues.

Peak Current Mode Control (PCMC) offers improved closed-loop bandwidth and stability margin, excellent line regulation and audio-susceptibility, compared to Voltage Mode Control (VMC) [11]. Controller reconfiguration in DCMC provides scopes for further improvement, thus making it an attractive choice in mainstream power converter circuits. Over the last decade, significant research efforts have been attempted to develop simple yet effective DCMC techniques [1]–[6]. The predictive PCMC in [1] considers uniform current loop sampling and predicts the inductor current using the information of system parameters. An uniformly sampled DMC was developed in [2], which considers a virtual ramp compensation throughout. A mixed-signal PCMC was developed in [3,4], in which the voltage controller utilizes digital implementation and the current loop remains in the analog domain. Sensorless DMC was reported in [6]. Unlike in digital VMC which exhibits limit cycle oscillations mainly due to quantization effects [7,8], DCMC is primarily affected by selection of current-loop sampling rate as discussed below.

A. Fast-scale instability in uniform current loop sampling

Consider a dc-dc buck converter governed by the DCMC as shown in Fig. 1. Assuming a constant current reference $i_{\text{ref}}$, it can be shown that the control input $u$ (in Fig. 1) always gets saturated if $f_{c,s} = f_s$ (uniform sampling). However, an addition of a compensating ramp can restore a regular on-off operation as shown in Fig. 2(a). Let $i_n$ and $i_{n+1}$ represent the sampled values of the inductor current $i_L$ at the beginning and the end of the $n$th clock period. With an analog compensating ramp of slope $m_c$, the discrete-time current dynamics (sampled) over the clock interval $T$ becomes

$$i_{n+1} = i_n + (m_1 + m_2) d_1 T - m_2 T,$$
$$d_1 = (i_{\text{ref}} - i_n) / (m_1 + m_c) T,$$
$$i_{n+1} = (1 - a) i_n + (a i_{\text{ref}} - m_2 T),$$
$$a = (m_c - m_2) / (m_1 + m_c),$$

where $m_1$ and $m_2$ represent rising and falling slopes of $i_L$.

For unperturbed $i_{\text{ref}}$, zero-input stability of current-loop can be analyzed by considering partial derivative $\partial i_{n+1}/\partial i_n$ of (1), and the stability condition can be derived as $|1 - a| < 1$. Taking into account the discretization effect in the compensating ramp (Fig. 2(a)), the discrete-time duty ratio $d_n$ becomes

$$d_n = \Delta d_n \times \text{ceil}(d_1 / \Delta d_n); \quad \Delta d_n = t_{\text{clk}} / T.$$ (2)

Replacing $d_1$ by $d_n$ in (1), the closed-loop discrete-time current dynamics can be derived, which would result in discontinuity and Taylor series cannot be applied. However, zero-input stability of the perturbed current dynamics can be intuitively perceived in the local sense around $i_n = i_{\text{ref}}$ as

$$|\partial i_{n+1}/\partial i_n|_{i_n = i_{\text{ref}}} = (1 - a).$$ (3)

From (1) and (3), local stability of the sampled current dynamics (around $i_n = i_{\text{ref}}$) seems to remain unaffected by discretization. However, it is very important to investigate existence of a periodic solution (period-1 fixed point over the period $T$) under DCMC with finite current-loop sampling. From (3), period-1 fixed point for an analog ramp, $i^{*}_{p,1,a}$ is

$$i^{*}_{n+1} = i^{*}_{n} = i^{*}_{p,1,a} = i_{\text{ref}} - m_2 T / a.$$ (4)

From (1) and (2), error in duty ratio, $\xi_d = d_n - d_1$, becomes

$$\xi_d = \text{ceil}(x) - x \Delta d_n = \text{frac}(x) \Delta d_n; \quad x = d_1 / \Delta d_n.$$ (5)
The error $\xi_d$ is bounded by $\Delta d_n > \xi_d \geq 0$. For an initial current $i_n$, $\xi_d$ causes an error in the final current as

$$i_{\xi, n+1} = (m_1 + m_2) \xi_d.$$  
(6)

For a non-zero $\xi_d$, period-1 orbit will never exist in DCMC using discrete-time ramp compensation; however, for $\text{frac}(x) = 0$, there exists a stable period-1 orbit if $|1 - a| < 1$. A non-zero duty ratio error results in sub-harmonic oscillation as shown in Fig. 2(a), which increases ripple parameters and leads to EMI problems. Error in the current ripple can be reduced by decreasing clock period $t_{clk}$. However, this increases clock frequency requirement and word-length size of the Digital Pulse Width Modulator (DPWM). A limiting case $\lim_{t_{clk} \rightarrow 0}$ tends to force $\lim_{\xi_d \rightarrow 0}$, which is practically not feasible to achieve.

### B. Instability in multi-sampled current loop

Considering the buck converter under DCMC, Fig. 2(b) shows current waveform for the current-loop sampling frequency, $f_{c,s} = N \times f_s$, where $N$ is a positive integer greater than unity. Without ramp compensation, the discrete-time duty ratio $d_n$ remains the same as in (2) with $\Delta d_n = 1/N$ and $m_c = 0$. Similarly, duty ratio error $\xi_d$ and current error $i_{\xi, n+1}$ can be formulated. It can be shown that a non-zero duty ratio error results in sub-harmonic oscillation as shown in Fig. 2(b). A further increase in $N$ reduces error bound, which requires an ultra-fast A/D converter with substantial power consumption. This paper attempts to compute the steady-state duty ratio in real-time using an moving average filter while the closed-loop controller is in action. A Time-to-Digital Converter (TDC) generates an equivalent digital code which enforces a virtual open-loop configuration at steady-states.

This paper attempts to compute the steady-state duty ratio in real-time using an moving average filter while the closed-loop controller is in action. A Time-to-Digital Converter (TDC) generates an equivalent digital code which enforces a virtual open-loop configuration at steady-states. This disables current-loop sampling and controller computation, thereby saving substantial power and eliminating sub-harmonic oscillations.

### II. DUTY RATIO COMPUTATION IN DCMC

#### A. Working principle of the proposed scheme

Fig. 1 shows a dc-dc buck converter governed by the DCMC along the proposed control, where $C(z)$ implies a discrete-time compensator. The output of $C(z)$, $v_c[n]$ is used as one of the inputs to a Multiplexer (MUX), where the other input $v_d[k]$ is being generated by the ‘duty ratio computation’ block (Fig. 3). The signal $v_{CL}[n]$ represents the sampled inductor current $i_L[k]$ along with an optional compensating ramp $v_r[k]$. In this proposed DCMC, an active high Direct Duty Control (DDC) command is introduced (in Fig. 1). If $\text{DDC} = 1$, a DDC command is issued, which (i) connects the output of the MUX $v_{up}[n]$ to $v_d[n]$, (ii) disables the sampling clock for the current-loop A/D converter, and (iii) can also disable the controller computation. This enforces a virtual open-loop configuration.
and the computed duty ratio guides the buck converter. If $DDC=0$, the closed-loop DCMC is restored as shown in Fig. 1.

**Time-to-digital converter:** The TDC in Fig. 4 translates cycle-by-cycle duty ratio information into an equivalent digital code $v_T[n]$. The switching clock $f_{clk}$ and complement of the control signal ($u$) act as start and stop inputs for the counter. At the rising-edge of $f_{clk}$, the counter gets incremented at every rising edge of $f_{clk}$ until $u$ becomes low. The counted value is loaded to the register at the rising edge of $f_{clk}$ and after a short delay, the counter is reset to zero (in Fig. 4). The counter output can be directly used as a compensating ramp $v_i[k]$. The counter stops counting throughout rest of the switching cycle after $u$ goes low. This helps in saving power over a conventional counter-based ramp generator which gets incremented throughout the switching period. The stored value $v_T[n]$ represents an equivalent digitally coded duty ratio for the running PWM cycle with the resolution $\Delta d_n = t_{clk}/T$.

![Fig. 4. Time-to-digital converter in DCMC as highlighted in Fig. 1.](image)

**Duty ratio computation:** While $DDC=0$, primary objective of the ‘duty ratio computation’ block is to compute $v_T[n]$ in real-time by taking running average of $v_T[n]$ using a moving average filter as shown in Fig. 3. Filter order $N$ can be reconfigured based on design requirements. If the error voltage $v_e$ remains within $v_{up} > v_e[n] > v_{low}$ for $m$ consecutive (PWM) clock periods, the ‘waiting time’ block issues the DDC command, i.e., $DDC=1$ as shown in Fig. 3. Then the converter operates by the computed duty ratio in a virtual open-loop configuration. In case $v_e$ cannot remain within the hysteresis band for the specified number of cycles, an additional ‘dead-time generation’ block can also issue a DDC command after a finite number (say $m$) of switching cycles, in which $m$ can also be programmed. An active DDC command enables any further activity of ‘clock’ (internal clock of the ‘duty ratio reconstruction’ block in Fig. 3), thereby preventing any further update in $v_T[n]$. If there is any change in $2^n$ or higher LSB of $v_T[n]$ or in the voltage hysteresis band because of occurrence of a transient or due to the error in duty ratio computation, then $DDC=0$. This restores the closed-loop DCMC operation using the discrete-time controller after an integrator reset.

**B. Steady-state duty ratio computation:**

A PID controller can be considered as the discrete-time compensator $C(z)$ as shown in Fig. 1, and its output $v_{c[n]}$ under uniform voltage-loop sampling can be written as

$$v_{c[n]} = k_p v_e[n] + k_i T \sum_{k=0}^{n-1} (v_e[k] - v_e[n-1])/T, \quad v_{int[n]} = v_{int[n-1]} + v_e[n],$$

(7)

where $v_e[n]$ indicates sampled error voltage; $k_p$, $k_i$, and $k_d$ indicate proportional, integral, and derivative gains, respectively.

A common clock $f_{clk}$ is used for generating digital coded duty ratio $v_T[n]$ of the control signal $u$ as well as the compensating ramp $v_i[k]$. Thus duty ratio resolution $\Delta d_n = t_{clk}/T$ and ramp slope $m_c = q/t_{clk}$, where $q$ indicates voltage quantization level. Under closed-loop control, the ‘duty ratio computation’ block computes $v_T[n]$ by averaging digitally coded duty ratio $v_T[n]$ over $N$ switching cycles (in Fig. 3). The closed-loop discrete-time duty ratio $d_n$ can be derived using (2) by substituting $i_{ref} = v_T[n]$. For a $N$-sample averaging filter, the computed duty ratio $d_c[n]$ can be written as

$$d_c[n] = \frac{q t_{clk}}{T} \text{ceil} \left[ \frac{1}{N} \sum_{k=0}^{N-1} v_T[n-k] \right].$$

(8)

Thus accuracy of the computed duty ratio can be improved by increasing filter order and/or clock frequency of the TDC.

**C. Design of the proposed methods:**

In a buck converter with $v_{max}$ as an input upper voltage limit, resolution of $d_c[n]$ maps DPWM voltage resolution as

$$\Delta v_{DPWM} = v_{max} \times \Delta d_n.$$  

(9)

The voltage resolution of the ADC, $\Delta v_{ADC}$ is written as

$$\Delta v_{ADC} = v_{max}/2^m,$$  

(10)

where $m_1$ is the ADC bit-size. In conventional DPWM converters, the constraint on voltage resolution, $v_{DPWM} > v_{ADC}$, results in limit cycle oscillation, which may be further degraded after incorporation of inductor current samples in DCMC. In this proposed DCMC, the DDC command (i) eliminates voltage resolution requirement, thereby simplifying DPWM architecture, (ii) eliminates sub-harmonic oscillations because of virtual open-loop operation, and (iii) expands range of controller gains, thereby facilitating (off-line) controller design as well as (online) auto-tuning. Design of a compensator in PCMC can be carried out using continuous-time transfer functions with frequency domain specifications [13]. Thereafter, an equivalent discrete-time compensator can be derived using bilinear transformation [14]. Additional phase lag that would result from the effect due to zero-order-hold under finite sampling and the computation delay must be taken into account before implementing the discrete-time controller to meet desired phase margin and bandwidth. Finally the proposed scheme eliminates sub-harmonic oscillations, if at all exist, due to finite current-loop sampling and quantization.

Consider a periodic sub-harmonic oscillation using DCMC with $\{-2\Delta d_n, -\Delta d_n, 0, \Delta d_n, 2\Delta d_n, \Delta d_n, 0, \ldots\}$ as the periodic sequence of perturbed duty ratio around its nominal value $d_{nom}$. Taking 8-sample average, perturbation in $d_c[n]$ is

$$d_c[n] = \Delta d_n/8 (2^{-1} + 0 + 1 + 2 + 1 + 0 + 1 - 0) = 0.$$  

(11)

For the above periodic behavior, it can be shown that $d_c[n] = 0$ for any sequence of operation. Considering 4-sample averaging with $-\Delta d_n$ as the starting value, $d_c[n] = 0.5\Delta d_n$. Because of finite duty ratio resolution, $d_c[n]$ needs to be rounded to
further, it can be shown that magnitude of $\Delta d[n]$ will not exceed $\Delta d_{\text{in}}$ and $\Delta v_{\text{DPWM}}$ in (9) can give an estimate of maximum worst-case steady-state error. A larger $N$ and a smaller $t_{\text{clk}}$ would certainly improve steady-state errors, however, at the cost of higher memory and computational requirements. A design trade-off can be made by considering acceptable voltage error under worst-case sub-harmonic oscillations.

D. Compensation under duty ratio saturation:

In the TDC block, the magnitude of $v_T[n]$ is limited by the counting limits as shown in the (in Fig. 4) to ensure $0 \leq d[n] \leq 1$. Under duty ratio saturation while operating using the closed-loop DCMC, if $v_c[n]$ considerably deviates from its limits, real-time duty ratio computation may result in considerable errors. Such errors may accumulate in subsequent cycles. If a DDC command is issued, this will take $v_c$ outside the limits and reactivates the closed-loop controller.

Errors due to duty ratio saturation can be minimized by (i) inserting a saturation nonlinearity in the PID controller, (ii) increasing TDC clock frequency, thereby improving duty ratio resolution $\Delta d_{\text{in}}$, (iii) increasing filter order $N$, thereby smoothing out errors, and (iv) reconfiguring controller parameters to ensure (unsaturated) linear operation under closed-loop operation. A trade-off can be made using the above options to arrive an (hardware) resource-optimized solution.

III. HARDWARE IMPLEMENTATION

A buck converter prototype is made, and the proposed control is implemented using a Vertex-5 FPGA kit. The parameter set for the power circuit is as $f_s = 200$ kHz, $L = 10 \mu$H, $C = 470 \mu$F, $i_0 \in [0.3 \ A, 4 \ A]$, $v_{\text{ref}} = 8 \ V$, and the nominal reference voltage $v_{\text{ref}} = 3.3$ V. Frequency of the digital controller clock $f_{\text{clk}} = 100$ MHz. For the prototype signal conditioning circuits, two 8-bit pipeline ADCs (AD9280) are considered. The first one is for sampling the output voltage at the same rate of the switching frequency $f_s = 200$ kHz. The other one is for sampling the inductor current with a sampling rate $f_{c,s} = 200$ kHz for the uniform current-loop sampling and $f_{c,s} \in [1 \ MHz, 20 \ MHz]$ for the multi-sampled current-loop. A digital PI controller is considered for all test cases.

1) Load Transient Performance: Figs. 5 and 6 demonstrate load transient response for a step change in load current from 0.3 A to 3 A, and back with following axis properties. For above test results from the top, Ch. 1, Ch. 2, Ch. 3, and Ch. 4 indicate inductor current (2 A/div), output voltage (1 V/div), the computed duty ratio clock (10 V/div), and the DDC command (5 V/div), respectively. Fig. 5 is related to multi-sampled DCMC with $f_{c,s} = 10$ MHz, and 4-sample averaging is used for duty ratio computation. Fig. 6 relates to uniformly-sampled DCMC with ramp compensation, in which 8-sample averaging is used. The former results in faster transient response (settling time smaller than 20 $\mu$s) compared to that of the latter (of nearly 55 $\mu$s settling time) with less than 100 mV voltage undershoot/overshoot. The computed duty ratio using 8-sample averaging in Fig. 6 changes slowly compared to 4-sample averaging in Fig. 5. After the ‘duty ratio computation’ block issues a DDC command, the TDC block freezes stored $v_T[n]$ in the register; thus no more changes in $v_c[n]$ are allowed as long as the DDC command remains active. As a result, the computed duty ratio clock becomes fixed, which drives the buck converter in a virtual open-loop configuration and eliminate sub-harmonic oscillations.
using the open-loop DCMC with \( f_{c,s} = 50 \times f_s \), load step frequency (of 2.7 A step-size) can reach up to \( f_s/4 \). However, the proposed controller would require a few more cycles (based on the filter order) for accurate duty ratio computation before a DDC command can be issued, for example, 2 more cycles using 4-sample averaging. For a larger load step-size, the settling time drastically increases. In such cases, this additional cycle requirement using the proposed method would have insignificant impact on the closed-loop bandwidth.

2) Tracking Performance: Figs. 7 and 8 demonstrate transient performance for a step change in reference voltage from 1.6 V to 2.7 V, and back using 4-sample averaging. The same (magnitude) axis properties of Ch 2 and Ch 4 in Fig. 5 are retained here; however, those of Ch. 1 and Ch. 3 change to 5 A/div and 5 V/div, respectively. Both the cases are tested at \( R = 5 \Omega \) using the multi-sampled DCMC with \( f_{c,s} = 10 \text{MHz} \), however, at different input voltage conditions, \( v_{\text{in}} = 8 \) and 5 V for Figs. 7 and 8, respectively. The former results in 0.22 ms and 0.12 ms settling times for the reference step-up and step-down transients with 7.5 A and 9 A current overshoot and undershoot respectively. The proposed controller correctly computes both the steady-state duty ratios 0.2 and 0.3375, and the DDC command ensures near ideal open-loop operations. In Fig. 8, the closed-loop DCMC controller results in 0.24 ms and 0.12 ms settling times for the reference step-up and step-down transients with 6 A and 8.3 A current overshoot and undershoot, respectively. Both the steady-state duty ratios 0.32 and 0.54, are correctly computed and the DDC command ensures sub-harmonic free near ideal open-loop operations.

3) Performance Evaluation: Using the nominal power circuit parameters, efficiency of the converter was tested at 3 A load current using the uniformly-sampled DCMC. Using the closed-loop controller, measured efficiency was found to be 82%, which was improved to 86% after a DDC command was issued. Presence of sub-harmonic oscillations in former case increases the current ripple which significantly increases conduction losses. Sub-harmonic oscillations in multi-sampled DCMC can be minimized by increasing the current-loop sampling rate and introducing a ramp compensation. The former linearly increases power consumption of the ADC with the sampling rate, as evident from the datasheet of AD9280. The later degrades closed-loop bandwidth and stability margin as the DCMC would approach towards VMC with continuous increase in the ramp slope. However, the proposed method retains advantages of existing DCMC techniques, and the proposed DDC command ensures sub-harmonic free operation.

IV. Conclusions

This paper proposed a technique to compute steady-state duty ratio in real-time during a closed-loop operation in digital current mode control. A time-to-digital converter generates digitally coded duty ratio at steady-states using a moving average filter. Thereafter, a virtual open-loop operation was enforced which eliminates sub-harmonic oscillations and disables current-loop sampling and controller computation, thereby saving substantial power. Tests results demonstrated considerable accuracy in voltage regulation for a buck converter. Duty ratio saturation issues were discussed.

REFERENCES