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Abstract—Dynamic voltage scaling (DVS) is a useful technique to optimize performance and efficiency of CMOS digital processors using DC-DC converters that require to meet extremely fast slew rate demand. However, there exit conflicting design criteria in existing DVS power supply architectures. This paper proposes a single-inductor multi-output level (SIMOL) buck converter for low power DVS-enabled systems. Under the time optimal voltage transition recovery, the proposed architecture (i) achieves the performance much beyond system’s physical limits compared to conventional synchronous and multi-phase buck converter-based architectures, and (ii) can overcome conflicting power circuit design criteria in existing architectures. A comparative study is shown to evaluate the usefulness of the proposed architecture over the existing approaches under frequent voltage transitions. A prototype single-inductor four-output-level buck converter is tested and the performance improvements are demonstrated using test results.

I. INTRODUCTION

Dynamic voltage scaling (DVS) is widely acknowledged as one of the most effective techniques in saving power in low-power embedded processors for mobile applications, IoT devices, wireless sensor networks, automotive applications, and variety of portable devices [2], [3]. This approach is useful in optimizing the trade-off between the performance and the efficiency. In a CMOS digital processor, the dynamic power consumption is formulated as

\[ P_{\text{dyn}} = C_{\text{eff}}v_{dd}^2f_{\text{clk}}/2, \]  

where \( f_{\text{clk}} \) and \( v_{dd} \) indicate clock frequency and supply voltage, and \( C_{\text{eff}} \) is the effective capacitance including the activity factor. A DVS scheme saves energy that a linear reduction in the supply voltage leads to approximately a linear increase in its computational time while the power can be decreased in a quadratic manner. Thus the performance and efficiency trade-off can be met by dynamically varying the supply voltage [4]. A real-time scheduler assigns different processor voltage levels to tasks based on processor-induced energy optimization and processor technologies [5]. The power supply needs to change the voltage levels accordingly to meet the deadlines while reducing the dynamic power consumption.

A DC-DC converter is employed in scaling the supply voltage of a DVS-enabled system [1], which requires to meet an extremely fast slew rate demand. A synchronous buck converter is generally used for DVS applications [6]– [8]. A non-inverting buck-boost converter can be used when the input and output voltages are close to each other [9]. The use of linear PWM control is not sufficient to meet the fast slew rate demand. Time optimal control (TOC) achieves the fastest possible performance [10]– [12]; however, the settling time and the peak current are still limited by the physical limits of a DC-DC converter [13]. Methods of converter augmentation can achieve ultra-fast response [14]– [16]; however, such possibilities are not very useful for a voltage transition. A multi-phase buck converter can speed up transient recovery [17], [18]; however, their exists conflicting design requirements for existing topologies in Fig. 1 while attempting to reduce time and energy overheads under load and reference step transients. Single-inductor-multiple-output converters are used in DVS applications [19]– [21], which are used to power analog and digital supply rails.

It was reported in [22] that the energy utilization can be improved in a digital processor by supplying through quantized voltages over a fixed voltage, which can be further improved by using a variable DC voltage. Design issues for DVS-enabled processors are discussed in [23]. Considering quantized voltage levels, a single-inductor-multi-output-level (SIMOL) buck converter-based DVS architecture is proposed in this paper for low power DVS-enabled systems [1]. The proposed topology can achieve high resolution DVS and significantly reduce the time and energy overheads compared to existing topologies as shown in Fig. 1.

The paper is organized as follows: Section II introduces the...
proposed converter and discusses its practical aspects. Section III formulates the DVS transient overheads under TOC. Section IV presents a comparative framework for existing solutions and the proposed one. Section V discusses design and implementation issues. Section VI presents hardware implementation and experimentally justifies the merits of the proposed solution. Section VII concludes the paper.

II. THE PROPOSED BUCK-DERIVED DVS POWER SUPPLY
A. Schematic of the proposed DVS power supply

Figure 2 shows the schematic of the proposed single-inductor multi-output level (SIMOL) buck converter. The inductor and load are connected in the same way in a classical buck converter; however, instead of a fixed output capacitor, a bank of parallel capacitor modules are considered in the proposed architecture. Each module consists of a capacitor in series with a switch cell. Individual capacitors are pre-charged with different discrete voltage levels, and only one capacitor can be connected to the load at any point of time. At steady-state, this resembles a buck converter with \( S_m \) as the controllable switch. In this paper, four output capacitors, \( C_1, C_2, C_3, \) and \( C_4 \) are considered as shown in Fig. 2, which are pre-charged to the voltage levels \( v_1, v_2, v_3, \) and \( v_4 \), respectively. In a typical DVS-enabled real-time processor, these four quantized voltage levels correspond to resting, nominal, sprint, and super-sprint modes [24]. The processor load can be switched to any of the pre-charged capacitors. Thus, the output voltage can be changed with negligible time and energy overheads by utilizing the stored inductor and capacitor energies. In existing topologies (in Fig. 1), the total energy needed by a bulky capacitor during a voltage transition is supplied by the source via the output inductor. This limits the slew rate and increases the current overshoot, thereby increasing time and energy overheads [1].

B. Required quantized voltage levels

The number of required quantized voltage levels are dictated by the DVS-enabled processor scheduler. The latter attempts to optimize the processor energy utilization using quantized voltage levels, and a finite set of discrete voltage levels seem to be reasonable for this purpose [23], even considering the standby mode. It is expected that a better performance/efficiency trade-off can be achieved by using a finer voltage resolution [22], [27]. However, for this purpose using the proposed architecture (in Fig. 2), it is not recommended to further increase the output capacitor bank, as this would penalize the power density. Alternative solutions are discussed below:

1) Two-step method: Any arbitrary desired voltage level can be reached in two steps: Connect the processor load to the nearest available voltage level which is higher than the desired voltage level. Thereafter, the controller enables an additional step-down reference transient in order to reach the desired voltage level. In this method, the transient step-size can be reduced, compared to a synchronous buck converter; thus both the time and energy overheads can be reduced.

2) Voltage-dithering method: A voltage dithering method in [22] uses discrete voltage levels as shown in Fig. 3. This is a practical DVS solution in a low power CMOS-processor which must accommodate a wide range of logic (supply) voltage levels for optimal energy savings by minimizing dynamic power [28], [29]. Consider that a task requires a voltage level of 1.3 V which is not readily available in the proposed architecture. This voltage can be achieved by time multiplexing between two nearest available voltage levels using a PWM technique. In this case, available voltage levels 1.15 V can be used for 40% duration of the task deadline and 1.4 V can be used for the remaining duration. Referring to Fig. 3, the use of a lower voltage \( v_1 \) eventually increases the critical path time [30] in a DVS-enabled CMOS device which may likely to miss a real-time deadline. This would eventually result in reduced performance and blue screen issues. Thus a minimum voltage level of \( v_{d1} \) or higher will be needed to meet the deadline.

Voltage dithering requires fast transient performance while changing between the two voltage levels. Interestingly, this requirement can be perfectly anticipated by this proposed architecture which achieves ultra-fast voltage transition by utilizing pre-energized inductor current and pre-charged capacitor voltage. Thus, without using extra capacitors, a finer voltage resolution can be realized using the above methods alongside reduced time and energy overheads. Throughout rest of this paper, the voltage-dithering method is primarily considered.

C. Selection of MOSFETs for the capacitor bank

For the parallel capacitor bank in Fig. 2, consider that the pre-charged voltage levels of the output capacitors are maintained as \( v_1 < v_2 < v_3 < v_4 \). Thus it is apparent that a single
N-channel MOSFET would be enough for the highest pre-charged voltage level \(v_4\) with the drain connected to the capacitor \(C_4\). Similarly, a single NMOS would be enough for the lowest voltage level \(v_1\) with the source connected to the capacitor \(C_1\). This makes sure that the current flowing through \(C_4\) and \(C_1\) to the other capacitors can be completely blocked simply by turning off the MOSFETs \(S_4\) and \(S_1\), without the need of back-to-back MOSFETs. However, back-to-back MOSFETs are needed for the intermediate voltage levels \(v_2\) and \(v_3\) to completely block current flowing through \(C_2\) and \(C_3\) even when \(S_2\) and/or \(S_3\) are turned off. This is because of the body diode of the MOSFET which can provide a closed path.

In the hardware prototype, N-channel MOSFETs with part number IPB096N03LG are used, and from the manufacturer’s datasheet, the forward voltage of the body diode is found in the range of 0.9 V-1.2 V. However, it is found using PSPICE simulation that the leakage current starts flowing through the body diode when the source-to-drain voltage exceeds 0.5-0.6 V. This might start discharging the capacitor even when it is disabled. Thus back-back MOSFETs using (IPB096N03LG) devices for the intermediate voltage levels may be avoided if the voltage differences \((v_3-v_2)\), \((v_3-v_2)\), \((v_2-v_1)\) in Fig. 2 are smaller than 0.5 V for the given application. The other alternative for IC implementation may be the use of PMOS switches and tying the bulk to the highest voltage in the circuit by using dynamic body biasing [31]. This prevents body diode conduction, and body effect, which may eliminate the need for back-back MOSFETs.

The output voltage levels in low power DVS-enabled applications are in the range of 0.6-3.3 V. Thus the gate overdrive \((V_{GS} - V_{th})\) is not sufficient to reduce the on-state resistance \(r_{ds,ON}\) of a PMOS switch. This increases the on-time resistance, thereby increasing the ESR and output impedance using the proposed architecture. For the same on-state resistance and voltage rating, the size of PMOS is nearly 2-3 times larger than NMOS. Also being more expensive, the choice of PMOS devices depends on the application specifications.

It is apparent from Fig. 2 that the MOSFET’s on-time resistance \(r_{ds,ON}\) would eventually increase the ESR of the output capacitor in this proposed solution. It is well known that the figure of merit of a power MOSFET is the product of its on-time resistance \(r_{ds,ON}\) and the gate-charge \(Q_G\). Compared to the input-side MOSFETs \((S_m, S_m)\), the output-side MOSFETs \((S_l, S_l)\) operate at a much lower frequency with the required voltage-transition rate decided by a DVS-enabled processor scheduler. Thus, inexpensive MOSFETs (NMOS) can be selected for the bank of output capacitors with lower \(r_{ds,ON}\) and higher \(Q_G\). The output impedance can be further reduced by considering multiple low-cost ceramic capacitors in parallel. While individual capacitors remain active, the respective MOSFETs would carry only the capacitor current. Thus the sizing of the switches would be simple, even if back-to-back switches are needed. Further, additional conduction losses are reduced, irrespective of load current conditions.

D. Gate drive requirements for the power MOSFETs

A half-bridge driver (part number HIP-2101) is used for the NMOS power switches \((S_m, S_m)\) at the input side, and a dedicated high side bootstrap driver (part number LTC4440ES6) is used for the output switches. For back-to-back MOSFET pairs \(S_2\) and \(S_3\), a common source configuration is used, and a single high side driver is used for each pair. High side drivers are used for the other single MOSFET pairs \(S_1\) and \(S_4\). Alternatively, charge pumps [32] and self-boosted snubber circuits [33] can be used to drive high side MOSFETs, and the design may be optimized for IC implementation.

E. Dead-time circuit and processor parasitic

Similar to a traditional buck converter, in this proposed topology, a dead-time circuit is needed for the input-side MOSFETs \((S_m, S_m)\) to prevent any shoot through current. Additionally, a dead-time circuit is used for the output-side MOSFETs in order to avoid activation of two successive switches while the processor load is switching between the respective capacitor terminals. During a small portion of the dead-time, the processor load may be completely disconnected from the capacitor bank, and the processor’s parasitic capacitance or load capacitance \(C_p\) in Fig. 2 attempts to maintain the output voltage regulation. Thus it is important to speed up MOSFET recovery time for minimizing the dead-time or to consider an additional fixed parasitic capacitance \(C_p\) in parallel to the processor, provided that the effective \(C_p\) must be considerably smaller than the output capacitors, \(C_1\) to \(C_4\). In the prototype, 1 \(\mu\)F parasitic capacitance is considered with a dead-time of 30 ns. \(L_p\) in Fig. 2 is the printed circuit board (PCB) trace inductance (typically around 2 nH). It protects from high \(di/dt\) between the output capacitors and the load parasitic capacitance \(C_p\) while the load is switching between the respective capacitor terminals. For low power on-chip implementation, the capacitor size can be further reduced to achieve high power density.

F. Various practical aspects

1) Charging of output capacitors: During the start-up, all the capacitors are sequentially charged using a sequence of burst pulses; thereafter, the processor load is connected to individual capacitors as per requirements.

2) Leakage charge compensation: During run-time, any capacitor may get discharged through the leakage path if it remains disconnected for a longer duration, and the rate of discharge depends on its time constant. The time constants of individual unloaded capacitors are primarily determined by their insulation resistances \(r_{ins}\). These are typically around 1 \(M\) \(\Omega\) which can be found in the manufacturers’ datasheet; thus the time constants are in the order of few seconds. Thus the voltage level would fall below a threshold value \(v_{th}\) if a capacitor continues to remain disabled for more than 10,000,000 consecutive switching cycles. Then the capacitor requires leakage charge compensation that can be anticipated simply by extending the voltage dithering technique. A capacitor with a higher pre-charged voltage level requires a higher \(v_{th}\). For
each capacitor with a pre-defined voltage level, $v_{th}$, may be customized based on its time constant.

Leakage charges can be compensated by activating individual capacitors at least once within their respective time constants. This can be easily achieved using the voltage dithering method in Fig. 3, which allows one to periodically connect individual capacitors with the inductor and the processor load.

Consider a case study using the proposed topology in Fig. 3 with available voltage levels 1.4 V, 1.15 V, 0.9 V, and 0.7 V. Suppose 1.3 V is needed by a processor to finish a task within the deadline; however, this voltage level is not readily available. As discussed in Sec. II-B2, voltage dithering can be applied for the task using the 1.4 V level for 60% duration and the 1.15 V level for the remaining duration. Alternatively, the same task can be executed using the 0.9 V level for 20% duration and the 1.4 V level for the remaining duration. Compared to the later, the difference in voltage levels is smaller for the former; thus time/energy overheads may be reduced using nearest voltage levels. However, the later can be used on demand if the 0.9 V voltage level requires leakage charge compensation. This requirement is infrequent and only be executed in case of leakage compensation. Thus, voltage dithering can be used for leakage charge compensation. If a voltage dithering is not recommended for charge compensation, an auxiliary power-efficient compact circuit would be needed, which remains a future challenge.

III. FORMULATION OF DVS TRANSITION OVERHEADS UNDER TIME OPTIMAL CONTROL

A. DVS system requirements and practical constraints

A DVS scheme involves assigning different voltages to tasks based on task scheduling algorithms. Figure 4 shows the output voltage of a DC-DC converter which undergoes a reference voltage transient to meet a dynamic voltage transition while supplying a DVS-enabled processor. The output voltage needs to change from $v_{ref1}$ to $v_{ref2}$, and back to complete the task-I and task-II within the allotted deadlines of $D_1$ and $D_2$ cycles, respectively. An ideal voltage-transition requires an immediate voltage change in a real-time processor, which does not incur any time and energy overheads as shown in Fig. 4.

The physical limits in a DC-DC converter result in a finite settling time (time overhead) and an overshoot/undershoot in the inductor current (energy overhead). In general a voltage transition needs to be initiated much earlier than expected so as to make it available for the processor, when it is actually needed. This requires information of the start and end times of a task along with its voltage level well in advance. Thus it is important to have interactions between the processor scheduler and the power supply. Modern digital devices allow communication among the processor and the power supply unit in the digital form. This can provide detailed information of the sequence of tasks along with the estimated start and end times, energy requirements, etc [16], [25]. In such cases, prior voltage information can be used to initiate a dynamic voltage transition using a DC-DC converter preceding the tasks as shown in blue trace in Fig. 4. During this DVS transition, the processor operates at a higher voltage than required by a task. This would finish the task well before the deadline, keeping the processor idle for a considerable amount of time. This would increase both the dynamic and static power consumptions of a CMOS processor, which eventually degrades the utilization factor. Thus a DVS-slew rate of 1 V/µs or higher [23] is needed to finish intensive real-time tasks within deadlines and to increase the efficiency of the processor, while reducing time and energy overheads.

In the rest of this paper, a framework is developed under time optimal transient recovery to analytically formulate the time and energy overheads of various DVS power supply architectures, including the proposed solution.

B. Formulation of time overheads

The time overhead $T_o$ is primarily the measure of the finite settling time in a DC-DC converter in response to a dynamic voltage transition as shown in Fig. 4. Thus finite settling times are formulated for existing and the proposed buck-derived under the consideration of time optimal transient recovery.

1) Synchronous buck converter: Figure 5 shows the transient response of a synchronous buck converter for a step change in reference voltage. The capacitor current ($i_C$) slopes are assumed to be the same as those of the inductor current with the rising slope $m_1$ and the falling slope $m_2$. Using capacitor charge balance, the settling time $T_s$ and the peak current $i_{pk}$ for a step-up transient can be obtained as [1]

$$i_{pk} = \sqrt{\frac{2CL\Delta v_{ref}(v_{in} - v_{ref1})}{v_{ref1}},}$$

$$T_s = t_1 + t_2 = \sqrt{\frac{2LC\Delta v_{ref}}{v_{in} - v_{ref1}} v_{ref1}.}$$
It is clear from (2) that for a reference step-size $\Delta v_{\text{ref}}$, the settling time can be improved by decreasing either the inductor $L$ or the capacitor $C$. However, a decrease in $L$ increases both the peak and the ripple current. Further, a decrease in $C$ would increase the voltage undershoot/overshoot during a load step transient. The detailed derivations can be found in [1]. Similar arguments are equally applicable for a reference step-down transient. Thus, above physical limits and conflicting design criteria pose power-circuit design challenges for a synchronous buck converter for DVS applications.

2) Multi-phase buck converter: For a multi-phase buck converter, all the inductors need to be activated during a large-signal recovery to achieve the fastest slew rate under time optimal control (TOC). Thus the effective inductance $L_{\text{ef}}$ for a four-phase buck converter under TOC becomes one-fourth of its individual values, i.e., $L_{\text{ef}} = L/4$. Similarly, for an $N$-phase buck converter, the effective inductor value, assuming all the inductors to be identical (with a value $L$), becomes $L_{\text{ef}} = L/N$. Hence, the rising and the falling slopes of the capacitor current become $m_{1,\text{ef}} = N \times m_1$ and $m_{2,\text{ef}} = N \times m_2$. The waveforms under step-up voltage transition is similar to those shown in Fig. 5 using the effective inductor as $L/N$. Thereafter, analytical expressions of the settling time and the peak current in (2) can be extended for an $N$-phase buck converter, with the updated slopes. Using (2), the peak current $i_{\text{pk,mult}}$ and the settling time $T_{\text{s, mult}}$ for a four-phase buck converter can be formulated as [1]

$$T_{\text{s, mult}} = t_1 + t_2 = T_s/\sqrt{N}, \quad i_{\text{pk,mult}} = i_{\text{pk}}/\sqrt{N}. \quad (3)$$

Above expressions show that the settling time and peak inductor current per phase can be improved by using a multi-phase buck converter by a factor of $\sqrt{L_{\text{ef}}/L} = 1/\sqrt{N}$, compared to that in (2).

3) Proposed topology: A reference transient in the proposed architecture is similar to a load transient in a conventional synchronous buck converter, with a load step-size $\Delta v_{\text{ref}}/R$ ($R$ being the load resistance) as shown in the Fig. 6. The average inductor current changes partially in the order of $\Delta v_{\text{ref}}/R$. As the load switches between capacitor terminals, the pre-energized inductor is connected to a pre-charged capacitor. Thus the processor can be connected to the desired output voltage almost instantaneously, with a small voltage deviation because of a load transient with a step-size $\Delta v_{\text{ref}}/R$. Thus the settling time, peak current, and voltage undershoot can be derived considering a similar load (step-up) transient event in a buck converter [1], which are as follows

$$T_{\text{s,load}} = \frac{\Delta i_o L}{(v_{\text{in}} - v_{\text{ref}})} \left(1 + \sqrt{\frac{v_{\text{in}}}{v_{\text{ref}}}}\right), \quad i_{\text{pk,load}} = \Delta i_o \sqrt{\frac{v_{\text{ref}}}{v_{\text{in}}}}$$

$$\Delta v_1 = \frac{\Delta v_{\text{ref}}^2 L}{2(v_{\text{in}} - v_{\text{ref}}) C}, \quad (4)$$

where $T_{\text{s,load}}$ is the settling time, $i_{\text{pk,load}}$ is the peak current, and $\Delta v_1$ is the voltage undershoot during a load step transient. Similarly, for a multi-phase buck under load transient, the settling time and the peak current can be derived using the same analogy in Sec. III-B2 as

$$T_{\text{s,load,mult}} = \frac{T_{\text{s,load}}}{\sqrt{N}}, \quad i_{\text{pk,load,mult}} = \frac{i_{\text{pk,load}}}{\sqrt{N}}. \quad (5)$$

For the proposed scheme, the load step size $\Delta i_o = \Delta v_{\text{ref}}/R$ and $v_{\text{ref}} = v_{\text{ref1}} + \Delta v_{\text{ref}} = v_{\text{ref2}}$ following a transition from $v_{\text{ref1}}$ to $v_{\text{ref2}}$. Thus, the settling time ($T_{\text{s, proposed}}$), the peak current ($i_{\text{pk,proposed}}$), and the voltage undershoot $\Delta v_{1,\text{proposed}}$ can be obtained from (4) as

$$i_{\text{pk,proposed}} = \frac{\Delta v_{\text{ref}}}{R} \sqrt{v_{\text{ref2}}}, \quad T_{\text{s, proposed}} = \frac{T_{\text{s,load}}}{R(v_{\text{in}} - v_{\text{ref2}})} \left(1 + \sqrt{\frac{v_{\text{in}}}{v_{\text{ref2}}}}\right) \quad (6)$$

$$\Delta v_{1,\text{proposed,undershoot}} = \frac{\Delta v_{\text{ref}}^2 L}{2(v_{\text{in}} - v_{\text{ref2}}) R^2 C}, \quad (7)$$

Similarly, during a step-down voltage transition as shown in Fig. 6(b), the load step size $\Delta i_o = \Delta v_{\text{ref}}/R$ and $v_{\text{ref}} = v_{\text{ref2}} - \Delta v_{\text{ref}} = v_{\text{ref1}}$ following a transition from $v_{\text{ref2}}$ to $v_{\text{ref1}}$.

$$i_{\text{pk,proposed}} = \frac{\Delta v_{\text{ref}}}{R} \sqrt{1 - \frac{v_{\text{ref2}}}{v_{\text{in}}}}, \quad T_{\text{s, proposed}} = \frac{T_{\text{s,load}}}{R(v_{\text{ref1}})} \left(1 + \sqrt{\frac{v_{\text{in}}}{v_{\text{ref1}}}}\right) \quad (7)$$

$$\Delta v_{1,\text{proposed,overshoot}} = \frac{\Delta v_{\text{ref}}^2 L}{2v_{\text{ref1}} R^2 C}, \quad (7)$$

It is clear from (6) and (7) that the peak current and the settling time depend only on the desired quantized voltage level $v_{\text{ref2}}$ or $v_{\text{ref1}}$ and the step size $\Delta v_{\text{ref}}$, and remains unaffected by the choice of the output capacitance. The latter only affects the voltage undershoot/overshoot. Thus, the same design criteria which are needed to reduce the settling time and voltage/current undershoot/overshoot under a load step transient are equally applicable.

The proposed topology can improve DVS performance compared to buck as well as multi-phase buck converters. However, load transient performance still remains the same as that using a conventional buck converter. Hence, it is apparent that the multi-phase buck will offer faster load transient recovery. For low power processors, the typical slew rates vary from 1 A/μs-10 A/μs for a load step change from 1 A to 6 A (TI PMICs TP554880, TPS54810). Interestingly, this slew-rate requirement can be met by a simple buck converter using the proximate time-optimal tuning [36]. Thus for such applications, the proposed architecture would be a better
solution over existing topologies as it also supports ultra-fast DVS slew-rate requirements.

C. Formulation of transient energy overhead

In a DVS enabled system, the energy overhead is induced simultaneously by the DC-DC converter and the processor. Various factors which contribute to energy overheads are analytically derived below.

1) Converter-induced energy overhead: The parasitic resistances, such as the DC resistance ($r_L$) of the inductor, the effective series resistance ($r_C$) of the capacitor and the ON-state resistance ($r_{ds,ON}$) of the MOSFETs, are primarily responsible for energy overheads. The energy overhead due to $r_L$ is given as

$$E_{inductor} = \int_{0}^{T_s} i_{swH}(t) r_L dt - \frac{v_{ref1}^2}{R^2} T_s.$$  

(8)

The energy overhead due to $r_C$ is formulated as

$$E_{capacitor} = \int_{0}^{T_s} \frac{i_{swL}^2(t)}{r_C} dt$$  

(9)

The overhead due to the ON-state resistances of high side and the low side MOSFETs for a synchronous DC-DC converter is obtained as

$$E_{HS} = \int_{0}^{T_s} i_{swH}(t) r_{ds,ON} dt - \frac{v_{ref1}}{R^2} D^2 T_s.$$  

(10)

$$E_{LS} = \int_{0}^{T_s} i_{swL}(t) r_{ds,ON} dt - \frac{v_{ref1}}{R^2} (1 - D)^2 T_s.$$  

(11)

where $i_{swH}, i_{swL}$ are the high side and low side switch currents respectively, and the duty ratio $D = (v_{ref1}/v_{in})$. Thus, the total energy overhead induced by the converter $E_{conv}$ becomes

$$E_{conv} = |E_{inductor}| + |E_{capacitor}| + |E_{HS}| + |E_{LS}|.$$  

(12)

Additional energy overhead in the proposed architecture due to the ON-state resistances of the switch cell $S_k$ need to be taken into account, which is formulated as

$$E_{Sk} = \frac{2E_{capacitor}}{r_C} r_{ds,ON,S_k}.$$  

(13)

where $E_{Sk}$ is the energy overhead due to the switch cell $S_k$, and $k=(1,2...,n)$ corresponds to the active cell (connected to the processor) at the given instant.

2) Processor-induced energy overhead: The widely known processor model [26] is given as

$$P_{proc} = C_p v_p^2 f_p + \alpha_1 v_p + \alpha_2$$  

(14)

where $P_{proc}$ is the total processor power consumption, $C_p$ is the average switching capacitance per cycle, $\alpha_1$ and $\alpha_2$ are processor constants, and $v_p$ and $f_p$ are the supply voltage and the clock frequency of the processor respectively. Thus, the energy overhead induced by the processor during a step-up voltage transition $E_{proc,up}$ is given as

$$E_{proc,up} = \int_{0}^{T_s} \left( C_p v_o^2(t) f_s + \alpha_1 v_o(t) + \alpha_2 \right) dt - E_{ideal}$$  

(15)

where $v_o(t)$ is the instantaneous output voltage evolving with respect to time. Similarly, the energy overhead induced by the processor during a step-down voltage transition $E_{proc,down}$ is obtained as

$$E_{proc,down} = \int_{0}^{T_s} \left( C_p v_o^2(t) f_e + \alpha_1 v_o(t) + \alpha_2 \right) dt - E_{ideal}$$  

(16)

where $f_s$ and $f_e$ are the clock frequencies before and after the voltage transition respectively. Thus, the total energy overhead induced by the processor $E_{processor}$ is

$$E_{processor} = |E_{proc}|$$  

(17)

The processor energy overhead in (17) gives an overall estimate of the total processor utilization. Increase in $E_{processor}$ significantly reduces the utilization factor and vice-versa.

The total energy overhead in a DVS enabled system is obtained from (12) and (17) as

$$E_{total} = E_{conv} + E_{processor}$$  

(18)

The total energy overhead for the existing buck-derived architectures and the proposed architecture is derived, by obtaining the time domain solutions of the $i_L, i_C, i_{swH}, i_{swL}$, and $v_o(t)$ and further, substituting these in (8)–(17).

IV. Figure-of-Merit: A Comparative Framework

A. Parameter set for comparative case studies

Consider the nominal parameter set for the proposed prototype as: $i_o \in [1 A, 7 A], v_{in} \in [5 V, 8 V], v_{ref} = 0.6 V - 3.3 V, L = 3.3 \mu H, C_1, C_2, C_3, C_4 = 320 \mu F, L_p = 2 \text{ nH}, C_p = 1 \mu F, the capacitor ESR r_{c1, c2, c3, c4} \cong 1 \text{ m}, the inductor DC resistance r_L \cong 1.8 \text{ m}, r_{ds,ON} \cong 9.6 \text{ m}, the power switches, r_{ds,ON,S_k} \cong 9.6 \text{ m} for the output MOSFETs, and the switching frequency $F_{SW} = 200$ kHz. For the analytical case study, the parameters of the processor are obtained from [26] as $f_p = 1.5 \text{ GHz} - 3 \text{ GHz}, C_p = 8.376 \text{ nF}, \alpha_1 = 36.3851, \alpha_2 = -33.9503$.

In this section, few case studies are considered for quantitative comparison of time and energy overheads using a synchronous buck converter and the proposed buck-derived...
DVS architectures. As the peak current requirements are different for individual topologies, the ratings of the inductor and power MOSFETs along with their sizes are expected to vary. For simulation study, the parameter set of a buck converter is as follows: $L = 3.3 \, \mu \text{H}, C = 320 \, \mu \text{F}, r_L \cong 4.1 \, \text{m} \Omega, r_c \cong 20 \, \text{m} \Omega, r_{\text{ds,ON}} \cong 5.7 \, \text{m} \Omega$. For the proposed converter, $L = 3.3 \, \mu \text{H}, C_1 = C_2 = C_3 = C_4 = 320 \, \mu \text{F}, r_L \cong 8 \, \text{m} \Omega, r_c \cong 20 \, \text{m} \Omega, r_{\text{ds,ON}} \cong 15 \, \text{m} \Omega$, and $r_{\text{ds,ON,Sk}} \cong 8.7 \, \text{m} \Omega$. The four quantized voltage levels chosen for simulation are 0.7 V, 0.9 V, 1.15 V, and 1.4 V. All the values used in the tables (I–VI) are obtained using the models which are analytically derived and also verified using simulation results.

### B. Comparative study of time and energy overheads

1) **Under available quantized voltage levels:** The fold of improvement in the settling time using the proposed scheme can be analytically derived using (2)–(6). Using the nominal parameter set in Sec. IV-A, time and energy overheads can be quantified for a step change in reference voltage from 0.9 V to 1.4 V and back at $R = 0.66 \, \Omega$ and $v_{\text{in}} = 6 \, \text{V}$. A comparative study of time overhead is shown in Table I, where $T_{o,\text{step,up}}$ and $T_{o,\text{step,dn}}$ represent settling time for step-up and step-down transients, respectively. This clearly indicates that the proposed scheme can achieve beyond time optimal performance over a synchronous buck converter.

<table>
<thead>
<tr>
<th>Time Overhead during a DVS Transition</th>
<th>Synchronous buck (µs)</th>
<th>Proposed buck (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{o,\text{step,up}}$</td>
<td>37.15</td>
<td>1.67</td>
</tr>
<tr>
<td>$T_{o,\text{step,dn}}$</td>
<td>31.36</td>
<td>5.79</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Energy Overhead during a Step-up DVS Transition</th>
<th>Synchronous buck</th>
<th>Proposed buck</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{\text{inductor}}$ (µJ)</td>
<td>6.74</td>
<td>0.0364</td>
</tr>
<tr>
<td>$E_{\text{capacitor}}$ (µJ)</td>
<td>16.9</td>
<td>0.0001</td>
</tr>
<tr>
<td>$E_{\text{HS}}$ (µJ)</td>
<td>1.2</td>
<td>0.0455</td>
</tr>
<tr>
<td>$E_{\text{LS}}$ (µJ)</td>
<td>8.26</td>
<td>0.0352</td>
</tr>
<tr>
<td>$E_{\text{Sk}}$ (µJ)</td>
<td>33.12</td>
<td>0.1199</td>
</tr>
<tr>
<td>$E_{\text{proc}}$ (µJ)</td>
<td>1000</td>
<td>1400</td>
</tr>
<tr>
<td>$E_{\text{total}}$ (µJ)</td>
<td>1034</td>
<td>140.13</td>
</tr>
</tbody>
</table>

Tables II and III compare the energy overheads using different DVS architectures, which clearly indicate that energy overheads can be significantly reduced using the proposed architecture compared to existing solutions.

2) **Voltage dithering:** The energy overheads are calculated for a step change in reference voltage from 0.9 V to 1.3 V at $R = 0.66 \, \Omega$ and $v_{\text{in}} = 6 \, \text{V}$. For the existing topologies in Fig. 1, this requires a reference transient. For the proposed topology, consider that this transition is from an available voltage level 0.9 V to another level 1.3 V which is not available. This target voltage level can be realized using the voltage-dithering method in Fig. 3. Consider below a study to compare energy overheads using various DVS architectures.

The controller initially selects 1.15 V to operate for 40 % duration of the task deadline and 1.4 V for the remaining duration. The overall energy overhead which involves two transitions (0.9 V to 1.15 V and 1.15 V to 1.4 V) is nearly 152.163 µJ. This is much smaller than 768.36 µJ using the synchronous buck converter. For a step-down transition from 1.4 V to 0.8 V, the energy overheads using the proposed topology is found to be 91.81 µJ, which is much smaller than 663.29 µJ using the synchronous buck converter.

3) **Capacitor count vs energy overhead:** Consider a required voltage transition from 0.7 V to 1.3 V needed by a task. Using the proposed architecture and the voltage-dithering method, a case study is shown below to demonstrate the trade-off between the number of capacitors and energy overheads.

(a) Using two capacitors with voltage levels 0.7 V and 1.4 V: The controller selects 0.7 V for 14.28% of the task, and thereafter transitions to 1.4 V and operates for rest 85.71% of task time. The energy overhead is found to be 188.71 µJ.

(b) Using four capacitors with voltage levels 0.7 V, 0.9 V, 1.15 V, and 1.4 V: The controller initially selects 1.15 V for 40% of the task time followed by 1.4 V for the remaining task time. The energy overhead is found to be 180.25 µJ.

(c) Using synchronous buck converter: For a step-up transition from 0.7 V to 1.3 V, the energy overhead using a synchronous buck converter is found to be 1400 µJ.

These indicate that the proposed topology substantially reduces the energy overhead. The number of output capacitors may be further reduced below four, and the voltage-dithering method can still be used to achieve a higher voltage resolution. However, this may increase energy overheads over a wide range, starting from standby to fully active modes. Thus there are scopes for optimization for a suitable trade-off between cost, size, and time/energy overheads.

### C. Comparative study of component ratings and sizes

A reduction in energy overhead implies a reduction in peak current; thus reduction in time and energy overheads provides opportunities to reduce size of the power circuit devices. Tables IV and V present possible peak ratings and footprints of the devices which can be chosen under different schemes.

<table>
<thead>
<tr>
<th>Energy Overhead during a Step-down DVS Transition</th>
<th>Synchronous buck</th>
<th>Proposed buck</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{\text{inductor}}$ (µJ)</td>
<td>2.17</td>
<td>0.0081</td>
</tr>
<tr>
<td>$E_{\text{capacitor}}$ (µJ)</td>
<td>1.08</td>
<td>0.001</td>
</tr>
<tr>
<td>$E_{\text{HS}}$ (µJ)</td>
<td>0.93</td>
<td>0.0036</td>
</tr>
<tr>
<td>$E_{\text{LS}}$ (µJ)</td>
<td>2.16</td>
<td>0.0528</td>
</tr>
<tr>
<td>$E_{\text{Sk}}$ (µJ)</td>
<td>0.017</td>
<td></td>
</tr>
<tr>
<td>$E_{\text{conv}}$ (µJ)</td>
<td>6.36</td>
<td>0.0833</td>
</tr>
<tr>
<td>$E_{\text{proc}}$ (µJ)</td>
<td>672.15</td>
<td>85.67</td>
</tr>
<tr>
<td>$E_{\text{total}}$ (µJ)</td>
<td>678.51</td>
<td>85.75</td>
</tr>
</tbody>
</table>
TABLE IV
RATING AND SIZE OF INDUCTOR(S): A COMPARATIVE STUDY

<table>
<thead>
<tr>
<th>Type</th>
<th>Total count</th>
<th>RMS current (A)</th>
<th>Saturation current (A)</th>
<th>Total board area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck</td>
<td>1</td>
<td>7.5</td>
<td>15-20</td>
<td>169</td>
</tr>
<tr>
<td>Proposed</td>
<td>1</td>
<td>7.5</td>
<td>10-12</td>
<td>100</td>
</tr>
</tbody>
</table>

TABLE V
RATING AND SIZE OF POWER MOSFET(S): A COMPARATIVE STUDY

<table>
<thead>
<tr>
<th>Type</th>
<th>Total count</th>
<th>Continuous drain current (A)</th>
<th>Pulsed drain current (A)</th>
<th>Total board area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck</td>
<td>2</td>
<td>7.5</td>
<td>30-120</td>
<td>16.8</td>
</tr>
<tr>
<td>Proposed</td>
<td>8</td>
<td>7</td>
<td>15-60</td>
<td>48</td>
</tr>
</tbody>
</table>

All the inductors can be selected SMD type, shielded with cut-tape packaging. Power MOSFETs can be chosen to be SMD type with TSOP package or the standard SOIC package. Because of reduced current rating of the MOSFET, microfet thin package can be used for the proposed topology. Above tables show that the overall board size can be reduced using the proposed scheme. However, the power density would be penalized because of using more number of output capacitors. However, SMD ceramic capacitors up to 330 µF, and 4 V are manufactured by MURATA, which significantly reduces the size. For low power applications, a smaller output capacitor can be used. Thus additional output capacitors along the switch cells using the proposed scheme does not significantly increase the size. Even these can be placed on-chip for further size reduction. This would make the proposed solution compact for low power applications, which can reduce the overall footprint because of using a smaller inductor.

D. Comparative study of steady-state power losses

Considering possible power circuit parasitics, Table VI compares the calculated steady-state power loss distribution for a synchronous buck converter and the proposed solution as shown in Fig. 2. The efficiency was calculated at the nominal power rating of 3 W, and the other parameters were obtained from the product datasheets. \( P_{\text{inductor}} \), \( P_{\text{capacitor}} \), \( P_{\text{HS}} \), \( P_{\text{LS}} \), \( P_{\text{sn}} \), \( P_{\text{switchloss}} \), \( P_{\text{bodydiode}} \), \( P_{\text{gate}} \), \( P_{\text{tr}} \), \( P_{\text{coss}} \), indicate buck high side MOSFET switching loss, body diode loss of the low side MOSFET, gate drive loss, body diode reverse recovery loss and buck MOSFETs output capacitance loss. \( P_{\text{total}} \) and \( P_{\text{output}} \) indicate total power loss and the output power respectively.

For the proposed solution, the additional output MOSFETs carry the ripple capacitor current while they remain connected with the processor load. Thus the proposed architecture has slightly lesser steady-state efficiency compared to a synchronous buck converter. The measured efficiency using the proposed buck converter is found to be 91.5% which is more or less consistent with the analysis.

E. Dynamic efficiency

Steady-state efficiency alone is not sufficient to fully characterize the overall energy efficiency of the converter. Thus it is important to consider dynamic efficiency in which energy and time overheads during a transient recovery can have significant impacts. It is apparent that smaller the time and energy overheads higher the dynamic efficiency, which is the primary objective of this proposed architecture.

The dynamic efficiency of the proposed topology and a synchronous buck converter are measured and compared in Fig. 7. The measured efficiency is obtained at a nominal power output of 3 W, with output voltage transition from 1.15 V to 1.4 V at \( R = 0.66 \) Ω and input voltage of 6 V. Fig. 7 shows that the dynamic efficiencies of both the converters degrade under frequent transients, which is consistent with the rule of thumb. However, superiority of the proposed converter in terms of dynamic efficiency becomes more prominent with increasing step-frequency over its conventional counterpart with an improvement of nearly 3 %. Thus, while penalizing the steady-state efficiency a little bit, the proposed SIMOL converter can significantly improve the overall efficiency under frequent transients by minimizing transient time/energy overheads.

V. DESIGN OF THE PROPOSED DVS ARCHITECTURE

The power supply design requirements for a DVS-enabled processor are to (a) minimize the settling time to meet...
the fast slew-rate demand, (b) to reduce the voltage undershoot/overshoot to be consistent with the logic voltage levels, and (c) to reduce the peak current to minimize ratings of the inductor and the switching devices. The final objective is aimed to minimize the inductor core size for a compact solution and to reduce the MOSFET gate capacitance, thereby reducing the switching losses.

For a DC-DC converter under a step load transient, the settling time can be reduced with the inductor, while the voltage undershoot can be reduced using a large capacitor. However, for existing buck and multi-phase buck converter-based DVS power supplies, conflicting conditions are found in (2), (3) under a step reference transient. These show that the settling time can be reduced with the inductor or the capacitor. However, the former increases the peak current while the latter increases the voltage undershoot/overshoot. Thus there exists conflicting design requirements for the power circuits using existing architectures (shown in Fig. 1).

A. Power circuit design based on regulatory requirements

Since the DVS load and the inductor \( L \) in the proposed architecture are connected only at one of the capacitor terminals at a time, this resembles a synchronous buck converter under steady-state conditions. During a voltage transition, the processor switches between the capacitor terminals, and the output voltage is brought to the desired steady-state level by utilizing stored energies in the inductor and the pre-charged capacitor. Thus, a voltage transition resembles a step load transient with a load step-size \( \Delta v_{ref} / R \). This enables the designers to unify both the reference tracking and the load transient requirements into simple regulatory requirements.

The design of the power stage follows a standard procedure \[35\]. The values of inductor and the capacitor are designed so as to meet the steady-state ripple specifications, and also the transient voltage overshoot/undershoot requirements as specified by the load. For the proposed prototype considered in this paper, all the output capacitors, \( C_1, C_2, C_3, \) and \( C_4 \), are chosen to have the same capacitance and ESR. Generally, individual output capacitors need to be selected based on their worst-case load current requirements. This helps in further optimizing the size of the power stage.

B. Digital current mode control for the proposed architecture

Figure 8 shows the closed-loop control of the proposed single-inductor-four-output level buck converter in Fig. 2. For the feedback control loop, a mixed-signal current mode controller \[34\] is used, where the error voltage is sampled at the same rate of the switching frequency of 200 kHz using ADC 1 so as for computation of the voltage controller \( G_e(z) \). The tuning method in \[36\] is used to achieve proximate time optimal recovery. This requires information of the load current which can be estimated from the processor scheduler.

C. Digital current mode control design

A simple proportional and integral (PI) controller is considered as the discrete-time voltage controller \( G_e(z) \). The load current is estimated using the DVS processor scheduler, and the use of load current feed-forward can achieve near load invariant regulation \[37\]. Thus a small (fixed) integral gain is sufficient to minimize the steady state error. Thus, the overall controller structure can be framed as \[36\]

\[
\sigma = k_p(v_{ref} - v_o) + k_i \int (v_{ref} - v_o)dt + (i_{o,est} - i_L), \tag{19}
\]

where \( k_p \) and \( k_i \) are the proportional and integral gains; \( i_{o,est} \) is the estimated load current; \( i_L \) indicates the inductor current. The tuning method in \[36\] is applied to analytically derive \( k_p \) and a small (fixed) integral is used. This method uses a mixed-signal current-mode architecture and a fixed-frequency modulator throughout; thus it is simple to implement. Also the transient performance can be further improved by incorporating additional energy paths \[14, 15\].

D. Implementation of leakage charge compensation

The proposed topology uses a single PI controller to regulate the output voltage. The optimal proportional gains related to various operating conditions can be computed off-line and can be stored using look-up-tables (LUT) in a digital device. An FPGA device is considered for the prototype purpose. Further, two possible approaches are discussed below for leakage charge compensation.

1) A time driven approach: Consider a counter which is incremented at every rising edge of the converter switching clock with time period \( T_s \). A master periodic pulse \( P_m \) is generated with a time period of 10,000 \( \times T_s \). Then \( P_m \) can be used to derive four periodic pulses \( P_{s1}, P_{s2}, P_{s3}, \) and \( P_{s4} \) with identical time periods of 2,500 \( \times T_s \). However, the derived pulses are equally shifted in phase, such that the rising edges of the master pulse \( P_m \) and the first derived pulse \( P_{s1} \) always appear together. The rising edges of the derived pulses \( (P_{s1}, P_{s2}, P_{s3}, P_{s4}) \) can be used as the interrupts for the respective output capacitors \( (C_1, C_2, C_3, C_4) \) to indicate the need for leakage charge compensation. Based on the status of an interrupt, the respective voltage level may be considered as part of the voltage dithering for the subsequent task. A conservative estimate is considered to select time
periods of individual pulses. These can be further optimized depending on time constants of individual output capacitors due to leakage resistance.

2) An event driven approach: This method requires periodic monitoring of individual capacitor voltages. Then a cost-effective multi-channel serial A/D converter with a slower sampling rate would be sufficient to digitize individual capacitor voltages using a time-multiplexed algorithm. If any capacitor voltage requires leakage charge compensation, that voltage level may be considered as part of the voltage dithering for the subsequent task.

A time-driven method is simple to implement, which completely relies on time periods of individual pulses. This technique does not require monitoring of all the capacitor voltages. As requirements for charge compensation are infrequent, this technique may not considerably affect the overall energy efficiency. On the other hand, an event-driven method requires extra signal conditioning circuits, and also the control method may be complex; however, it may be more reliable because of monitoring actual capacitor voltages. In the hardware prototype, a time-driven technique is considered for leakage charge compensation.

VI. HARDWARE IMPLEMENTATION

The proposed single-inductor-four-output-level buck converter prototype is fabricated, and the proposed controller is implemented using a Xilinx Virtex-5 FPGA device. The same prototype has been used for testing a conventional synchronous buck converter. The nominal parameter set in Sec. IV-A is considered for the experimental investigation. The time period of the FPGA controller clock is taken as $t_{clk} = 10$ ns. The components used for the power circuit are listed in Table VII. For the prototype signal conditioning circuits, a differential pipeline A/D converter (AD-9215) is considered for sampling the output voltage. The ADC uses a differential amplifier (AD-8138) to convert the single ended output voltage into differential form for the reduction of common mode noise. The output of the digital compensator $v_c[n]$ is added with the estimated load current $i_{o,est}$ (in Fig. 8). The output is then converted into an equivalent analog voltage $v_A$ by using a 12-bit D/A converter (AD-9762) followed by a differential amplifier (AD-8130). A high speed comparator (TLV-3501) is used to compare $v_A$ with the sensed inductor current $i_L$. The comparator output is then latched, and the dead-time circuit generates the respective gate signals. A 10 mΩ current sense resistor is used to sense $i_L$ followed by a current sense amplifier (LT 1999). Further a simple analog multiplexer (MAX 4638) is used to time-multiplex the terminal voltages.

Slightly over-rated discrete components are used for the laboratory prototyping. However, the design can be substantially optimized, and the cost can be reduced with fewer components for stand-alone and IC level implementation.

<table>
<thead>
<tr>
<th>TABLE VII</th>
<th>POWER CIRCUIT BOARD COMPONENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component</td>
<td>Part number</td>
</tr>
<tr>
<td>$S_m, S_m'$</td>
<td>IPB096N03L G</td>
</tr>
<tr>
<td>Inductor</td>
<td>IHLP8787MZER3R3M5A</td>
</tr>
<tr>
<td>$S_1, ..., S_4$</td>
<td>IPB096N03L G</td>
</tr>
<tr>
<td>Output caps</td>
<td>GRM31CR60J157ME11</td>
</tr>
<tr>
<td></td>
<td>GRM21BR61E106KA73L</td>
</tr>
</tbody>
</table>
For the test results in this paper, quantized voltage levels are taken over a wide range from 0.7 V to 3.3 V. Moreover, the choice of discrete voltage levels are completely flexible for the proposed architecture.

A. Transient performance

Figures 9 and 10 show the transient performance using the proposed buck and the synchronous buck converters for a step change in reference voltage from 1.8 V to 3 V and 1.4 V to 0.9 V respectively, at $R = 0.66 \Omega$ and $v_{in} = 6$ V. The performance under step-up and step-down transients is tabulated in Table. VIII. The proposed architecture nearly eliminates the peak current while interchanging the load resistance with $R = 0.66 \Omega$ among discrete voltage levels as shown in Fig. 9(a) and Fig. 10(a). However, there exist a small negligible undershoot and overshoot in the output voltage. The peak current using the mixed-signal current mode architecture can be kept within an upper limit for a synchronous buck converter; however, this would further increase the settling time as shown in Figs. 9(c) and 10(c). Thus the proposed scheme considerably reduces both the time and energy overheads without the need of a current limiter, compared to a synchronous buck converter.

Figure 9(a) shows the auxiliary capacitor current (with the current probe resolution of 5 A/V) in Ch. 3 and voltage in Ch. 4 related to 1.8 V and 3.3 V output levels respectively. This indicates that the capacitor carries ripple current only when it is active; otherwise, its voltage remains nearly constant.

B. Voltage dithering: A case study using available voltage levels

Consider that two tasks (Task 1 and Task 2) require voltage levels of 1.075 V and 1.15 V to finish within the allotted deadlines. Applying the voltage-dithering method in Fig. 3 in this proposed architecture, for the Task 1, 0.95 V is used for 50% of the task time and 1.2 V is used for the remaining duration as shown in Fig. 11. This can achieve the required voltage level 1.075 V in the average sense. A similar methodology is applied for the Task 2 which uses 1.35 V and 0.95 V voltage levels of equal durations. For both the cases, it is found that under frequent DVS transitions, the proposed technique can achieve high voltage resolution and ultra-fast response with negligible time and energy overheads.

C. Power circuit redesign from a regulator perspective

Figure 12 shows the transient response using the proposed topology for a step change in load current from 1.89 A to 6.6 A. This results in 18 $\mu$s settling time, 1.5 A (inductor) current overshoot, and 0.15 V (output) voltage undershoot. Since the proposed topology can be designed based on regulatory requirements, a larger capacitor can be used to further reduce the voltage undershoot. Figures 13 and 14 show the performance of the proposed topology and conventional synchronous buck converter respectively, under the simultaneous changes in reference voltage from 1.8 V to 3.3 V and load current from 1.89 A to 6.6 A at 6 V input voltage. The time overhead, voltage undershoot, and energy overhead are significantly reduced using the proposed solution. Thus both tracking and regulatory requirements can be transformed into a purely regulator design using the proposed architecture.

For all the test results using a higher $k_p$, sub-harmonic instability was found, even with duty ratio $d < 0.5$, because of finite sampling of the error voltage in presence of capacitor ESR [38]. Thus at steady state, an additional ramp compensation is used for stabilization.

D. Performance during dead-time between the output switches

Figure 15 shows the performance using the proposed topology during the dead-time between switching among the output capacitors. Figure 15 shows that using $C_p$ of 1 $\mu$F and 30 ns

<table>
<thead>
<tr>
<th>Table VIII: Comparison of Transient Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_s$ step-up ($\mu$s)</td>
</tr>
<tr>
<td>$i_{pk}$ step-up (A)</td>
</tr>
<tr>
<td>$T_s$ step-down ($\mu$s)</td>
</tr>
<tr>
<td>$i_{pk}$ step-down (A)</td>
</tr>
</tbody>
</table>

Fig. 11. Voltage dithering in the proposed architecture using quantized voltage levels at $R = 0.66 \Omega$ and 6 V input with $C = 320 \mu$F: Time scale - 20 $\mu$s/div.

Fig. 12. Proposed topology under a step change in load current from 1.89 A to 6.6 A for $v_{ref} = 3.3$ V, 6 V input and $C = 320 \mu$F: Time scale - 20 $\mu$s/div.
dead-time, the output voltage drops by nearly 40 mV with negligible ringing effects while changing the load (along with the inductor) from a lower capacitor voltage (of 1.15 V) to a higher capacitor voltage (of 1.4 V) level at $R = 0.66 \, \Omega$ and $v_{in} = 6 \, V$. A similar voltage drop is also found while bringing back the load to the earlier lower capacitor voltage level. This voltage-drop seems to be within an acceptable limit for a processor load, and there exist scopes for further improvement.

E. Adaptive voltage positioning (AVP)

Under steady state, the proposed topology would resemble a classical synchronous buck converter. Thus adaptive voltage positioning (AVP) is applicable in the proposed architecture. The test result in Fig. 16 demonstrate the feasibility to implement the AVP technique in this proposed topology. Fig. 16 shows a load step-up transient from 1 A to 6 A at $v_{in} = 6 \, V$. Time scale - 20 $\mu s$/div.

VII. Conclusions

In this paper, a single-inductor-multi-output-level buck converter based DVS architecture was proposed, which could achieve performance much beyond system physical limits of that using existing DVS architectures. Further, it is possible to achieve high voltage resolution using a voltage-dithering technique with negligible time and energy overheads. Comparative studies and test results demonstrated significant performance improvements over existing architecture with reduced time/energy overheads for low power DVS-enabled systems. The proposed architecture promises an energy-efficient solution for low power DVS enabled systems.

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REFERENCES


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