Parameter-Insensitive Mixed-Signal Hysteresis-Band Current Control for Point-of-Load Converters with Fixed Frequency and Robust Stability

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Abstract—The inductor current ripple under hysteresis current control is sensitive to system as well as controller parameters, which often deviates from the desired band. Thus a phase-locked-loop (PLL) is employed to regulate the switching frequency over the operating range. Digital platform drastically simplifies this using an all-digital PLL (ADPLL) and offers the controller-tuning flexibility for improved performance. However, the use of uniform voltage-sampling often leads to multi-limit cycle instability. This paper proposes a mixed-signal hysteretic current controller (MSHCC) with the digital voltage-loop and the analog current-loop. A digital-to-analog converter is sufficient to generate time-multiplexed current references. This achieves robust stability and parameter-insensitive current ripple by sampling the error-voltage at the rising edge of the high-side gate signal. Stability analysis is carried out using discrete-time models. The proposed MSHCC can be configured to either of the peak, average, or valley current-mode techniques along with the flexibility to adjust the switching frequency using an ADPLL for real-time energy-optimization. The proposed scheme is implemented using an FPGA device and tested on a buck converter prototype. The MSHCC scheme can be extended to a multi-phase buck converter.

Index Terms—Hysteresis current control, mixed-signal control, asynchronous sampling, parameter-insensitivity, robust stability.

I. INTRODUCTION

The ever increasing growth of digital devices facilitates high performance control implementation for point-of-load converters [1]– [8]. A mixed-signal architecture seems to be a promising solution, because of implementing the fast-changing inductor current in the analog domain [3]– [5]. This paper proposes a mixed-signal current hysteretic controller that addresses some longstanding issues in hysteresis control.

Hysteresis current control (HCC) offers (a) inherent current-loop stability and (b) current limiting, (c) fast transient response, and (d) good accuracy [9]– [24]. However, it suffers from serious practical problems [10], as discussed below.

A. Parameter sensitivity in an analog HCC technique

Figure 1 shows a buck converter schematic governed by an analog HCC scheme [9]. The control waveforms are shown in Fig. 2, assuming the output-voltage ripple \( \Delta v_o \) being dominated by the effective-series-resistance (ESR) of the output capacitor \( C \) and considering a proportional voltage controller, i.e., \( G_c(s) = k_p \) in Fig. 1. Consider \( v_o \) and \( v_c - \Delta i_H \) as the peak and valley current references in Fig. 2. The current ripple \( \Delta i_L \) and the time period \( T_h \) can be derived as

\[
\Delta i_H = \frac{\Delta i_H L}{(1 + k_p r_C)}, \quad T_h = \frac{v_{in} \Delta i_H L}{(v_{in} - v_o)(1 + k_p r_C}),
\]

where \( v_{in} \) is the input voltage. This shows that \( \Delta i_L \) in (1) is smaller than the desired hysteresis band \( \Delta i_H \). Moreover, \( \Delta i_L \) and \( T_h \) vary with the capacitor ESR and the controller gain. The time period \( T_h \) would also vary with the output capacitor, if the characteristics impedance can no longer be neglected [6]. Thus it is difficult to design an input filter using an HCC scheme, which eventually leads to EMI problems [10].
B. PLL/DLL-based frequency regulation in analog HCC

Prior research efforts in [9]–[18] have been attempted to regulate the switching frequency in HCC. Generally a phase-lock-loop (PLL) is considered to achieve a desired switching frequency by varying the hysteresis band. A direct hysteresis band adaptation technique in [14], [15] considers an analog PLL-based arrangement. This requires a frequency-to-voltage converter which increases analog component count, thereby increasing size and power loss along with a slower frequency-loop. A faster recovery can be achieved by using a digital PLL (DLL)-based architecture in [16]. However, beside using a time-to-digital converter (TDC), the use of a voltage-controlled resistor increases component count. A delay-line DLL-based approach in [17] enables ultra high-frequency implementation, and a comprehensive survey of PLL/DLL-based techniques can be found in [18]. The above approaches are primarily limited to an analog HCC scheme.

C. Existing digital/mixed-signal hysteresis control techniques

Digital/mixed-signal hysteresis control can simplify the frequency regulation method by considering an all digital PLL (ADPLL) [19], which also offers an auto-tuning flexibility for the feedback voltage controller [20]–[27]. A fully digital HCC scheme requires multiple A/D converters [22]. A mixed-signal solution seems to be a promising alternative [23]. However, a uniform output voltage sampling in an HCC scheme may exhibit undesirable multiple limit cycle oscillations [24], which is substantiated with a case study to follow.

1) Multi-limit cycle oscillation using uniform sampling:
Consider a set of power circuit parameters for the buck converter (in Fig. 1) as: \( C = 470 \mu \text{F}, R = 1 \Omega, v_{\text{in}} = 8.5 \text{~V}, R_{\text{C}} = 20 \text{~m}\Omega, \Delta I_{\text{H}} = 2 \text{~A}, \) and \( v_{\text{ref}} = 3.3 \text{~V} \). Consider a proportional-integral (PI) voltage controller with the proportional gain \( K_{\text{p}} = 50 \) and (continuous-time) integral gain \( K_{I} = 10000 \). For a voltage-loop sampling rate \( f_{\text{vs}} = 500 \text{kHz} \), Fig. 3 clearly shows instability using a clocked HCC scheme, whereas the analog HCC scheme remains stable. Fig. 4 shows that the output voltage is sampled using a uniform rate; however, switching events occur non-uniformly as per the hysteresis logic. The timing mismatch between sampling and switching points results in multi-limit cycle phenomena [24]. This increases ripple parameters, as evident from Fig. 3, and may lead to EMI problems. A higher sampling rate can reduce the timing mismatch, which requires a fast analog-to-digital converter (ADC) with increased cost and power loss.

2) Asynchronous sampling approaches: Asynchronous control methods are useful to minimize limit cycle oscillations [25]–[29]. The synchronous/asynchronous voltage-mode control in [25], [26] considers a digital-to-analog converter (DAC) to compare the reference signal with the output voltage. This was extended to mixed-signal current-mode control [27]. This uses an extra DAC for the current-loop; thus the number of DACs and analog comparators increases. Also finite quantization levels using a lower-bit DAC can considerably affect steady-state frequency regulation and cycle-by-cycle stability.

A flash ADC was used in [28], [29] to sample the output voltage \( v_o \) once per cycle. This synchronizes the closed-loop operation when \( v_o \) crosses a quantization level; however, noise in \( v_o \) may considerably affect the sampling process. Also the flash ADC increases size, power, and cost.

This paper proposes a mixed-signal hysteresis current control (MSHCC) scheme which can (i) be used with any ADC, (ii) reduce hardware and sampling resources, (iii) simplify control mechanism, (iv) achieve parameter-insensitive current ripple \( \Delta I_{\text{H}} \), (v) fast response, and (vi) robust stability.

This paper is organized as follows. Section II introduces the proposed MSHCC scheme. Stability analysis is carried out in Section III. Section IV discusses the design of the proposed scheme. Section V extends the proposed scheme to a multi-phase buck converter. Section VI presents hardware implementation using a synchronous buck converter. Sec. VII concludes the paper.

II. THE PROPOSED MIXED-SIGNAL HCC TECHNIQUE

Figure 5 shows the schematic of the proposed MSHCC scheme which primarily consists of three blocks: ‘timing circuit’, ‘real-time band adaptation’, and ‘dead-time circuit’. The former generates digital code \( v_T \) related to the instantaneous time period \( T_{\text{H}} \) using a counter and a system clock \( F_{\text{clk}} \). This also generates the sampling clock \( F_{\text{vs}} \) to sample the error voltage \( v_e \), which is detailed mechanisms will be discussed later. The digital voltage controller \( G_e(z) \) computes in synchronism with \( F_{\text{vs}} \); the outputs \( v_c[n] \) and \( (v_c[n] - \Delta I_{\text{H}}) \) represent the

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peak and valley current references. Only one comparator is used in this proposed scheme as shown in Fig. 5. Thus one DAC is sufficient to generate time-multiplexed current references using the high-side gate signal as the select line. The DAC output $v_D$ is directly compared with the inductor current in the analog domain.

**A. Dead-time circuit configuration**

Measurement noise and switching spikes may lead to chattering in the comparator output $u_c$. A dead-time circuit is used as shown in Fig. 6, which uses an ‘edge-triggered mono-shot circuit’ and a ‘dead-time generator’. The former identifies an active (either rising or falling) edge and triggers the mono-shot operation for ‘m’ consecutive clock periods using the system clock with the frequency $f_{clk}$. This stores the status of the comparator output at the beginning of the mono-shot operation and disables any further changes in the output $u_m$ throughout the duration $m/f_{clk}$. Since the MUX output changes with the status of $u_m$ (in Fig. 5), a smaller value of $m$ would be enough to avoid initial chattering. The ‘dead-time generator’ block attempts to avoid any shoot-through current, in which the adjustable delays should be optimized using timing parameters of the MOSFETs and the associated drivers.

**B. Real-time band adaptation using an ADPLL**

Figure 7(a) demonstrates control waveforms using the peak-current mode configuration, where $v_c[n]$ is sampled at every rising edge of $u_H$ and the current reference $v_c[n]$ remains constant throughout the periodic interval $T_{h1}$. Thus the inductor current ripple $\Delta i_1$ resembles the hysteresis current band $\Delta i_{h1}$. For a given time period $T_{h1}$, $\Delta i_{h1}$ at steady-state becomes

$$\Delta i_{h1} = \frac{\left( v_o (v_{in} - v_r) \right)}{L v_{in}} \times T_{h1}. \quad (2)$$

Referring to Fig. 5, $v_r$ is the digital code for $T_{h1}$ and generated using a TDC. The desired switching period $T_{d}$ can be achieved simply by setting the desired band

$$\Delta i_D = \frac{v_{Td}}{v_{T1}} \times \Delta i_{h1}, \quad (3)$$

where $v_{T1}$ and $v_{Td}$ are the TDC outputs for the respective time periods $T_{h1}$ and $T_{d}$ (related to the desired time period). Thus a fixed-frequency steady-state operation can achieved by adjusting $\Delta i_{h1}$ in real-time using (3). However, it would be difficult to implement a division operation using fixed-point implementation. While an iterative Newton-Raphson method can be used, this would require considerable hardware resources. A more straightforward method is to piecewise linearize the functional form $f(v_{T1}) = (v_{Td}/v_{T1})$ in (3), thereafter, multiplying by $\Delta i_{h1}$. Using a 10-bit TDC, $t_{clk} = 10\text{ns}$ for $F_{clk}$, and $v_{Td} = 500$ for the nominal switching frequency of 200 kHz, $v_{T1}$ is found to be $v_{T1} \in [350, 650]$ for the input voltage range $v_{in} \in [5\text{ V}, 9\text{ V}]$. Thus $f(v_{T1})$ can be approximated as

$$f(v_{T1}) \approx \begin{cases} 2.430 - 0.00286 \times v_{T1} & \text{for } v_{T1} \in [350, 499] \\ 1.744 - 0.00154 \times v_{T1} & \text{for } v_{T1} \in [500, 650], \end{cases} \quad (4)$$

where $v_{T1} \in I^+$. The above expression can be easily implemented using fixed point arithmetic. This requires a generalized adder/subtractor and a multiplier with two (fixed) discrete gains; thus multiplier-less multiplication algorithms can be used [30] to optimize hardware resources. The result in (4) is finally multiplied with $\Delta i_{h1}$ to compute the desired current hysteresis band in order to achieved a fixed frequency operation. This approach is adopted in this paper.

Alternatively, the TDC in this proposed MSHCC scheme enables one to implement an ADPLL algorithm [19], which
D. Synchronous/asynchronous controller computation

Figure 8 demonstrates computation of the discrete-time PI controller in synchronism with the time-multiplexed synchronous/asynchronous sampling clock $F_s$. This uses the synchronous clock $F_s$ during large-signal transients, and the event-driven clock $F_{H,G}$ for computing once per switching cycle during small-signal and steady-state conditions. This would be effective in saving real-time hardware resources, yet closely retaining the performance over a uniformly sampled discrete-time PI controller using the clock $F_s$ throughout [31].

E. Flexibility and real-time configurability

The proposed scheme in Fig. 5 shows a peak current mode controlled MSHCC scheme, in which the peak current is controlled by the outer voltage loop, while the valley inductor current is controlled using the hysteresis band $\Delta i_H$.

This can be configured in real-time to a valley current mode control scheme by using the control voltage $v_c[n]$ as the valley current reference, while $\Delta i_H$ will be added with $v_c[n]$ to generate the peak reference current. At steady-state, $v_c[n]$ will be sampled at every falling edge of $u_H$. The proposed scheme can be extended to an average current mode control scheme by simply changing the peak and valley current references (in Fig. 5) as $(v_c[n] + \Delta i_H/2)$ and $(v_c[n] - \Delta i_H/2)$. All other sampling and control mechanisms will remain the same as the peak-current mode control scheme.

III. A FRAMEWORK OF DISCRETE-TIME MODELING AND STABILITY ANALYSIS

A buck converter in Fig. 1 operating under continuous conduction mode (CCM) can take two feasible switch states, namely the MODE 1 when the high-side switch is ON and the MODE 2, otherwise. State-space models can be written as

$$\dot{x} = A_0x + (A_1x + Bv_{in})u + A_1(1-u), \quad v_o = C_0x, \quad (5)$$

where $x = [i_L, v_{cap}]^T$ with $i_L$ is the inductor current; $v_{cap}$ is the voltage across the capacitor; $v_o$ is the output voltage, and

$$A_0 = \begin{bmatrix} 0 & 0 \\ 0 & -R_o/RC \end{bmatrix}; \quad B = \begin{bmatrix} 1/L \\ 0 \end{bmatrix};$$

$$A_1 = \begin{bmatrix} 0 & -R_o/R_nC \\ (1/R_nC - R_o/L) \end{bmatrix}; \quad C_0 = \begin{bmatrix} R_n/C \\ R_n/RC \end{bmatrix};$$

where $R_o = R/(R + r_C)$. The control input $u = 1$ for MODE 1 and $u = 0$ for MODE 2. Thus the output voltage can be expressed as

$$v_o(t) = \frac{Rr_C}{(R + r_C)}i_L(t) + \frac{R}{(R + r_C)}v_{cap}(t). \quad (7)$$

Assuming linear inductor current dynamics and quadratic capacitor voltage dynamics, $i_L$ and $v_{cap}$ can be written as

$$i_L(t) = i_{int} + m_Lt;$$

$$v_{cap}(t) = v_{c,int} + \frac{(i_{int} - i_o)}{C}t + \frac{m_K^2}{2C}, \quad (8)$$

where $i_{int}$ and $v_{c,int}$ are the initial values of $i_L$ and $v_{cap}$, respectively; $i_o$ indicates the load current. The slope of the
inductor current, \(m_k\) can be written as

\[
m_k = \begin{cases} 
  m_1 = (v_{in} - v_o)/L & \text{during Mode 1} \\
  -m_2 = -v_o/L & \text{during Mode 2}.
\end{cases}
\]  

(9)

Using (8) and (9) into (7), the output voltage can be derived.

A. Discrete-time Modeling

Discrete-time models under fixed-frequency PWM are derived with respect to the switching clock; however, such a clock is not available in this proposed MSHCC scheme. Instead, a rising/falling edge of \(u_H\) is used to derive discrete-time models under different current-mode configurations.

1) Peak current-mode configuration: The control waveforms in Fig. 7(a) shows a rising edge of \(u_H\) is used as the sampling point using the peak current-mode configuration. Thus, the complete discrete-time model can be derived for the sequence consisting of the MODE 1 followed by the MODE 2. Let the inductor current and the output voltage at the start of the \(n^{th}\) switching cycle be \(i_n\) and \(v_n\), and those at the end of the clock period be \(i_{n+1}\) and \(v_{n+1}\), respectively.

Referring to Fig. 7(a), let \(i_1\) and \(v_1\) at the end of the MODE 1 be \(i_1\) and \(v_1\), which are derived using (7)–(9) as

\[
i_1 = i_n + m_1 t_h,
\]

\[v_1 = v_n + \frac{R}{R + r_C} \left[ \frac{r_C m_1 + i_n - i_o}{C} t_h + \frac{m_1 t_h^2}{2C} \right],
\]  

(10)

the initial output voltage \(v_n\) is obtained using (7) and (8) as

\[v_n = \frac{[RrCi_n + Rv_{c,n}]}{(R + rc)}.\]  

(11)

Considering the final conditions of the MODE 1 as the initial conditions of the MODE 2, the final conditions \(i_{n+1}\) and \(v_{n+1}\) of the \(n^{th}\) switching cycle can be derived using (7)–(9) as

\[i_{n+1} = i_n + \Delta i_{H},
\]

\[v_{n+1} = v_n + \frac{R\Delta i_{H}}{R + r_C} \left[ \frac{r_C (i_n + m_1 t_h - i_o)}{m_2 C} \frac{\Delta i_{H}}{2m_2 C} \right],
\]  

(12)

where \(v_{c,n}\) is the voltage-controller output as shown in Fig. 5. Assuming the output current \(i_o\) to be constant, the term \(i_n - i_o\) in (10) and (12) can be written as \(i_n - i_o = -m_1 t_h/2\). This indicates that any perturbation in \(i_n\) is immediately reflected in the instantaneous on-time \(t_h\). Thus the expression of \(v_{n+1}\) in (12) can be further simplified using (10) as

\[v_{n+1} = v_n + \frac{R}{R + r_C} \left[ \frac{r_C (i_n + m_1 t_h - i_o)}{m_1 C} \frac{\Delta i_{H}}{2m_1 C} \right],
\]  

(13)

where \(\alpha_1 = \frac{R}{(R + r_C)} \left[ \frac{r_C + \Delta i_{H}}{2m_1 C} \right].\)  

(14)

2) Valley current-mode configuration: Figure 7(b) shows the control waveforms under the valley current-mode MSHCC scheme, in which the switching cycle begins with the MODE 2, when the high-side switch is turned off. Thus a falling edge of \(u_H\) is used to sample the error voltage. Consider the \(n^{th}\) switching cycle with the time period \(T_h\) and the off-time \(t_o\). Let the inductor current and the output voltage at the start of the \(n^{th}\) switching cycle be \(i_n\) and \(v_n\), and those at the end of the clock period be \(i_{n+1}\) and \(v_{n+1}\), respectively. Let \(i_2\) and \(v_2\) at the end of the MODE 2 be \(i_2\) and \(v_2\), which are derived using (7)–(9) as

\[i_2 = i_n - m_2 t_h,
\]

\[v_2 = v_n + \frac{R}{R + r_C} \left[ \frac{r_C (i_n - i_o)}{C} \frac{m_2 t_h^2}{2C} \right].
\]  

(15)

Considering the final conditions of the MODE 2 as the initial conditions of the MODE 1, the final conditions \(i_{n+1}\) and \(v_{n+1}\) of the \(n^{th}\) switching cycle can be derived using (7)–(9) as

\[i_{n+1} = v_n + \Delta i_{H},
\]

\[v_{n+1} = v_n + \frac{R\Delta i_{H}}{R + r_C} \left[ \frac{r_C + (i_n + m_2 t_h - i_o)}{m_2 C} \frac{\Delta i_{H}}{2m_2 C} \right].
\]  

(16)

Assuming the output current \(i_o\) to be constant, the term \(i_n - i_o\) in (15) and (16) can be written as \(i_n - i_o = m_2 t_h/2\). This indicates that any perturbation in \(i_n\) is immediately reflected in the instantaneous on-time \(t_h\). Thus the expression of \(v_{n+1}\) in (16) can be further simplified using (15) as

\[v_{n+1} = v_n - \alpha_2 m_2 t_h + \alpha_2 \Delta i_{H},
\]  

(17)

where \(\alpha_2 = \frac{R}{(R + r_C)} \left[ \frac{r_C + \Delta i_{H}}{2m_1 C} \right].\)  

(18)

B. Stability Analysis using the Proposed MHS CC Scheme

Referring to Fig. 8, the output of the discrete-time PI controller \(G_c(z)\) in Fig. 5 can be written as

\[v_{c,n} = k_p v_{e,n} + u_1[n],\]  

(19)

\[u_1[n] = u_1[n - 1] + k_i v_{e,n},\]  

\[v_{e,n} = (v_{ref} - v_{n}).\]  

The discrete-time PI controller (19) uses the time-multiplexed synchronous/asynchronous clock \(F_{vs}\), and its implementation is shown in Fig. 8 with the discussion in Section II-D.

1) Stability analysis under peak current-mode MSHCC: Figure 7(a) shows the control waveforms under the peak current-mode MSHCC scheme. This considers the rising edge of the high-side gate signal, \(u_H\), for error voltage sampling and controller computation. It can be found from (12) that the current-loop exhibits unconditioned zero-input stability; thus the closed-loop stability is completely determined by the voltage-controller. Referring to Fig. 7(a), the on-time \(t_h\) during the \(n^{th}\) cycle can be derived as

\[t_h = \frac{v_c[n] - i_n}{m_1} = \frac{v_c[n] - v_c[n - 1] + \Delta i_{H}}{m_1},\]  

(20)

Using (13) and (20), the closed-loop discrete-time voltage equation can be derived; thereafter, the perturbed discrete-time model can be derived using (19) as

\[\hat{v}_{n+1} = [1 - (k_p + k_i) \alpha_1] \hat{v}_n + \alpha_1 k_p \hat{v}_{n-1}.\]  

(21)

It has been reported in [32] that Z-transformation can be applied on perturbed discrete-time maps of a DC-DC converter under a variable frequency operation. Applying Z-transformation on (21), the closed-loop characteristics equation can be obtained, and the eigenvalues become

\[\lambda_{1,2} = \frac{1}{2} \left[ 1 - (k_p + k_i) \alpha_1 \pm \sqrt{[1 - (k_p + k_i) \alpha_1]^2 + 4k_p \alpha_1} \right].\]  

(22)
Substituting the above equation into (17) and incorporating small perturbations, the perturbed closed-loop discrete-time voltage dynamics can be shown to be the same as that in (21), excepting \( \alpha_1 \) to be replaced by \( \alpha_2 \) in (18). The same stability condition in (24) can be used for the valley current-mode MSHCC scheme by replacing \( v_{\text{ref}} \) with \( v_{\text{in}} - v_{\text{ref}} \).

4) Stability analysis under average current-mode MSHCC: As discussed in Section II-E, the average current-mode MSHCC can be realized by simply changing the peak and valley current references (in Fig. 5) as \( (v_c[n] + \Delta i_H/2) \) and \( (v_c[n] - \Delta i_H/2) \). All other sampling and control mechanisms will remain the same as the peak current-mode MSHCC scheme in Section III-B1, and the on-time during \( n^{\text{th}} \) cycle can be derived as

\[
t_h = \frac{v_c[n] + (\Delta i_H/2) - i_n}{m_1} = \frac{v_c[n] - v_c[n-1] + \Delta i_H}{m_1}.
\]

From (20) and (26), it is clear that the on-time using the average current-mode MSHCC scheme is exactly the same as that using its peak current-mode version. Thus the closed-loop stability boundary would be the same as that in (24).

C. Effects due to the comparator delay

In the proposed mixed-signal CMC, an analog comparator is used to compare the reference current with the inductor current. Thus a finite comparator delay \( \tau_d \) is expected to exist. This would increase the effective on-time \( t_{\text{eff},n} \) (during the \( n^{\text{th}} \) cycle) of a constant off-time modulator as

\[
t_{\text{eff},n} = t_n + \tau_d.
\]

If \( \tau_d \) is assumed to be fixed, the perturbed discrete-time voltage dynamics in (21) will remain unaffected; thus the stability boundary in (24) will be retained under the proposed CMC.

IV. DESIGN OF THE PROPOSED MSHCC SCHEME

A. Static quantization requirements

Similar to a traditional mixed-signal current-mode control architecture [4], the proposed architecture uses an ADC for the digital voltage controller and a DAC for the analog current controller. Thus these two quantizers can make the proposed scheme prone to limit-cycle oscillations. From [4], the minimum DAC quantization requirement becomes

\[
M > \left\lfloor \log_2 \left( \frac{v_r}{\Delta v_{\text{adc}} K_s} \times \frac{2LF_h}{\sqrt{1 - 4D (1 - D)}} \right) \right\rfloor,
\]

where \( M \) is the number of bits of the DAC, and \( v_r \) is the DAC reference voltage; \( \Delta v_{\text{adc}} \) is the ADC voltage resolution [2]; \( K_s \) is the current sensor gain; \( F_h \) is the desired steady-state switching frequency using the proposed MSHCC technique.

B. High resolution frequency regulation using MSHCC:

Using the proposed MSHCC technique, an infinite duty ratio resolution can be achieved for the analog current controller; however, the resolution of the hysteresis current band \( i_H \) is...
limited by the DAC voltage resolution. This eventually results in a finite frequency resolution \( \Delta f_h \) as follows
\[
\Delta f_h = \frac{1}{N_h t_{clk}} - \frac{1}{(N_h + 1) t_{clk}} \approx \frac{1}{N_h^2 t_{clk}^2} \approx f_h \times \frac{1}{N_h}, \tag{29}
\]
where \( f_h \) indicates the nominal switching frequency for a nominal time period \( T_h = N_h t_{clk} \), and \( t_{clk} \) indicates the time period of the system clock \( f_{clk} \). Thus the frequency resolution can be improved by increasing \( N_h \), which requires a higher frequency system clock \( f_{clk} \).

C. Controller Design using Small-signal Modeling

An HCC technique is a typical example of non-linear control with a variable switching frequency; thus it is not straightforward to apply the state-space averaging technique. The circuit averaging technique using a PWM switch model was applied to an HCC scheme [33], and accuracy of the derived small-signal models was demonstrated using test results. In this proposed MSHCC, the current-loop is implemented in the analog domain; thus the expression of the control-to-output small-signal models was demonstrated using test results. In applied to an HCC scheme [33], and accuracy of the derived circuit averaging technique using a PWM switch model was demonstrated using test results. In this proposed MSHCC, the current-loop is implemented in the analog domain; thus the expression of the control-to-output small-signal models was demonstrated using test results.

Using the method of emulation, a discrete-time PI controller in (19) can be designed using the closed-loop block diagram as shown in Fig. 11. An equivalent analog PI controller, \( G_c(s) \) is considered using the discrete-time integral gain \( k_i \) and the sampling interval \( T_h \) which is the time period under the MSHCC scheme. An additional zero-order-hold (ZOH) circuit is considered for phase compensation due to the sampling delay, and a simplified rational transfer function \( G_h(s) \) is considered using a first-order Padé approximation as shown in Fig. 11. This ZOH equivalent for the digital voltage controller is applicable for a variable frequency operation if the perturbation is sufficiently small near the desired switching frequency [34]. Using the power circuit parameters in Sec. I-C1, the simulated loop-gain plot is shown in Fig. 12. This demonstrates that the closed-loop bandwidth of nearly 30 kHz for a nominal switching frequency of 200 kHz, the phase margin of 100 degree, and the closed-loop DC gain of 60 dB can be achieved for \( k_p = 50 \) and \( k_i = 0.9 \) in (19).

The bandwidth can be further improved by increasing the proportional gain \( k_p \); however, it is limited by the stability boundary in (24), which stimulates to investigate design methods to enhance the stability boundary.

![Fig. 11. Closed-loop block diagram of a synchronous buck converter using the proposed MSHCC technique: A small-signal perspective.](image)

\[
G_c(s) = k_i \frac{T_h}{k_i} + G_h(s) = \frac{R(1 + sr_C C)}{(1 + sT_h^2/2)(1 + sRC)}.
\]

D. Enhanced stability boundary using ramp compensation:

After the power-stage design, it is difficult to further reduce the capacitor ESR; thus an alternative method needs to be identified to extend the range of \( k_p \) in (24) for a stable operation. A compensating ramp can be easily generated using a counter, which needs to be subtracted from \( v_i[n] \) in the digital domain. The control waveforms in Fig. 7(a) are still applicable; however, the effective rising and falling slopes of the inductor current should be modified to \( 'm_1 + m_c' \) and \( 'm_2 - m_c' \), respectively. Thus the on-time \( t_{h,r} \) under ramp compensation during the \( n^{th} \) cycle can be derived using (20) as
\[
t_{h,r} = \frac{\Delta v_i[n_0] + \Delta i_{H}}{(m_1 + m_c)}, \quad \Delta v_i[n] = v_i[n] - v_i[n - 1]. \tag{31}
\]

Also the time period during the \( n^{th} \) cycle becomes
\[
T_{h,r} = \frac{\Delta v_i[n]}{(m_1 + m_c)} + \left[ \frac{m_1 m_2 - m_c (m_1 + m_2 - m_c)}{m_1 m_2 - m_c (m_1 + m_2 - m_c)} \right]. \tag{32}
\]

The final current \( i_{n+1} \) at the end of the \( n^{th} \) cycle becomes
\[
i_{n+1} = v_i[n] - (m_2 - m_c) (T_h - t_{h,r}) = v_i[n] - \Delta i_{H}. \tag{33}
\]

Similarly, the final output voltage \( v_{n+1} \) can be derived using (13) with the replacement of \( t_h \) by \( t_{h,r} \). This shows that the current-loop retains inherent zero-input stability, and the closed-loop stability can be carried out following the similar methodology in Sec. (III-B1). Thereafter, using (9), the stable gain range can be found to be
\[
(k_p + k_i) < \left( 1 + \frac{m_c}{m_1} \right) \times \left[ \frac{R + r_C}{R r_C} \right] \times \left[ 1 + \frac{L \Delta i_{H}}{2 r_C v_{ref} C} \right]^{-1}. \tag{34}
\]

Thus the controller gain range in (24) can be enhanced by a factor of \( (1 + m_c/m_1) \) by adding a compensating ramp; however, a larger value of \( m_c \) may degrade the bandwidth. Thus it should be carefully selected for a good trade-off between the performance and the stability boundary.

V. EXTENSION TO A MULTI-PHASE BUCK CONVERTER

The proposed MSHCC scheme can be extended to a multi-phase buck converter as shown in Fig. 13. Similar to a synchronous buck converter, the main phase is controlled using
A. Current-mode control of auxiliary phases

The sampling clock $F_{vs}$ in Fig. 8 is used as the master clock to generate phase-shifted reference clocks using the ‘phase shift circuit’ as shown in Fig. 14. Multiple time delay units are used with the delay $\Delta t_n = T_{th}/n_p$, the phase-shifted clocks are time-multiplexed with $F_{vs}$ using the select line $F_{flag}$ to generate switching clocks for auxiliary phases’ controllers. Thereafter, the current reference $v_A$ is used to implement analog current controllers for individual auxiliary phases, and the related timing diagrams are shown in Fig. 15.

B. Feasibility of realizing various current-mode configurations

As discussed in Section II-E, the proposed MSHCC scheme can be configured to either peak, valley, or average current-mode configurations. Thus similar configurations are also applicable for the auxiliary phases because of sharing the common current reference $v_A$. Interestingly, the average current-mode architecture can be implemented, without the need for sensing averaging inductor current, simply by setting the peak and valley current references for the main-phase MSHCC controller as $(v_c[n] + \Delta i_H/2)$ and $(v_c[n] - \Delta i_H/2)$, respectively. And the analog current reference $v_A$ accordingly adjusts the average current of all the phases. If needed, the current reference can be easily customized using the digital platform.

C. Time multiplexed operation of auxiliary phases

The MUX select-line $F_{flag}$ in Fig. 14 can be configured to use either phase-shifted clocks or the master clock $F_{vs}$ for individual phases. By setting $F_{flag}$ as $F_{sel}$ in Fig. 8, the transient response during a large-signal recovery can be accelerated by turning on all the phases simultaneously, thereby achieving the fastest slew rate. This would momentarily disable the phase-shift operation as long as $F_{flag} = F_{sel} = 1$. However, this would result in undesirable oscillations when the phase-shift circuit would be enabled again after the transient recovery, which is because of mismatches in initial currents of auxiliary phases [35]. Nevertheless, the proposed scheme provides the flexibility either to use phase-shifted clocks throughout or to use the master clock $F_{vs}$ during a large-signal recovery.

D. Open/closed-loop hybrid steady-state operation

In a practical multi-phase buck converter, a certain degree of mismatches can be expected in individual inductors and current sense resistances [36], [37]. The proposed MSHCC scheme allows one to implement the (steady-state) digital duty-ratio adjustment technique in [36] for auxiliary phases. In this case, apart from the time period, the digitally coded (steady-state) on-time, related to the main-phase, can be obtained from TDC of the MSHCC controller. This can be used with the phase-shifted switching clocks in Fig. 8 to generate the compensated open-loop gate signals for auxiliary phases, when the analog current controllers need to be disabled. During a large-signal recovery, the current controllers should be
restored for fast transient response. The asymmetric clocking in [37] is also possible using the proposed scheme by suitably delaying phase clocks for steady-state ripple minimization.

E. Phase shedding

A phase shedding method can be adopted using the proposed scheme by disabling some of the auxiliary phases and bypassing respective time delays in Fig. 8. Then the optimal phase algorithm in [38] can be realized to improve light load efficiency. In this case, the time delay \( \Delta n_p \) should be accordingly adjusted based on the number of active phases, and an adaptive windowing technique in [39] can be used to design the optimal switching frequency under light load.

VI. HARDWARE IMPLEMENTATION

A buck converter prototype has been made, and the proposed techniques are implemented using an FPGA device. The nominal power circuit parameters in Sec. I-C1 are considered here. The time period of the FPGA controller clock \( t_{c_{\text{clk}}} = 10 \text{ ns} \). A 10-bit differential pipeline A/D converter (AD9215) is used to sample the output voltage, which uses a differential amplifier (AD8138) for reduction in common mode noise. The digital controller output \( v_c[n] \) is converted into an analog voltage \( v_A \) using a 12-bit D/A converter (AD9762) followed by a differential receiver amplifier (AD8130). The output \( v_A \) is compared with the sensed inductor current using a high speed analog comparator (TLV3501). A shunt of 10 m\( \Omega \) is used to sense the inductor current followed by a high-side current sense amplifier (ADM4073) with a gain of 20. The nominal switching frequency is taken to be 200 kHz.

A. Steady-state behavior and spectral characteristics

![Figure 16](image1.png)

Fig. 16. Multi-limit cycle instability in a clocked HCC (in Sec. I-C1) with \( F_{vs} = 10 \text{ MHz} \) and \( \Delta t_{iv} = 2 \text{ A} \) at 8 V input: Time scale is 40 \( \mu \text{s/div} \).

1) Multi-limit cycle instability: Figure 16 shows the test result of a buck converter using the clocked HCC scheme as discussed in Sec. I-C1 at 3.2 A load current. Even using a high sampling rate \( F_{vs} = 10 \text{ MHz} \) for the A/D converter associated with the error voltage, this exhibits multi-limit cycle phenomena [24], and the FFT trace reveals an unpredictable power spectrum. Moreover, the inductor current ripple is much smaller that the current hysteresis band with \( \Delta i_{iv} = 2 \text{ A} \).

2) Stable operation using the proposed MSHCC: Figure 17 shows that the proposed MSHCC technique achieves a stable periodic operation. Because of using a fast comparator with a negligible time delay of nearly 4.5 ns, \( \Delta t_{iv} \) is more or less the same as that of \( \Delta i_{iv} \) with 1.2 A magnitude. The fundamental component of the FFT trace shows that the steady-state frequency varies a little bit around its nominal value of 200 kHz. This is primarily because of noise in the current sensor and the D/A converter output. However, the steady-state frequency variation was found to be within \( \pm 1\% \).

B. Load step-transient response:

Figures 18 and 19 demonstrate load transient performance of a synchronous buck converter using the proposed MSHCC scheme. Following design guidelines in Sec. IV-C and the stability requirement using (24), the controller gains are computed as \( k_p = 50 \) and \( k_i = 0.9 \). At 8.5 V input, Fig. 18 shows that the proposed MSHCC results in 8 \( \mu \text{s} \) settling time (nearly 2 switching cycles) and 50 mV voltage undershoot/overshoot for both the step-up and step-down transients. At 4.5 V input, Fig. 19 shows that the proposed MSHCC results in 15 \( \mu \text{s} \) settling time (3 switching cycles) and 120 mV voltage undershoot/overshoot for both the step-up and step-down transients.

A further increase in \( k_p \) would require a ramp compensation for a stable operation. It is interesting to notice that the closed-loop buck converter under the MSHCC technique remains stable for the both the load current and input voltage conditions. These are consistent with the analytical stability condition in (24) which is more or less insensitive to the input voltage and load current. Thus the improved performance can be retained over a wide operating range.

C. Reference step-transient response:

Using a higher proportional gain \( k_p = 100 \) and \( k_i = 0.9 \), Fig. 20 shows the transient performance of a synchronous buck converter using the proposed MSHCC technique. This shows near time optimal recovery for both the step-up and step-down transients. Moreover, the closed-loop converter remains stable for both the operating conditions. When the output voltage
reaches close to the reference command, a real-time band-adaptation algorithm in (3) is activated. This uses the fixed-point implementation in (4), and closely regulates the steady-state switching frequency for both the cases.

D. Feasibility of EMI reduction using the MSHCC scheme

The proposed MSHCC scheme allows the designer to customize the current hysteresis band \( i_{H} \). Recently, the proposed scheme has been extended to accommodate a periodic bi-frequency modulation technique in [40]. It was shown that the harmonic contents could be considerably attenuated by periodically modulating \( i_{H} \), while retaining the transient performance of the closed-loop converter. Further, using simplified ESR-dominated models, it was found that the same ESR-dependent stability boundary using the unmodulated MSHCC scheme would be applicable for the modulated MSHCC scheme. Thus it provides opportunities for further EMI reduction with the predictable ripple parameters. Also existing periodic and randomized modulation schemes in [41] can be easily implemented by modulating digitally coded \( i_{H} \).

VII. CONCLUSIONS

In this paper, a mixed-signal hysteretic current controller (MSHCC) was proposed. This considers a digital voltage controller and a D/A converter to generate (multiplexed) current references which are compared with the inductor current in analog domain. Robust stability and parameter-insensitive current ripple were achieved by using an asynchronous error-voltage sampling along with a fixed switching frequency using using the real-time band adaptation. The MSHCC achieves a fast recovery through tuning the digital voltage controller with inherent current limiting. The proposed scheme can be easily extended to a multi-phase synchronous buck converter.

REFERENCES


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