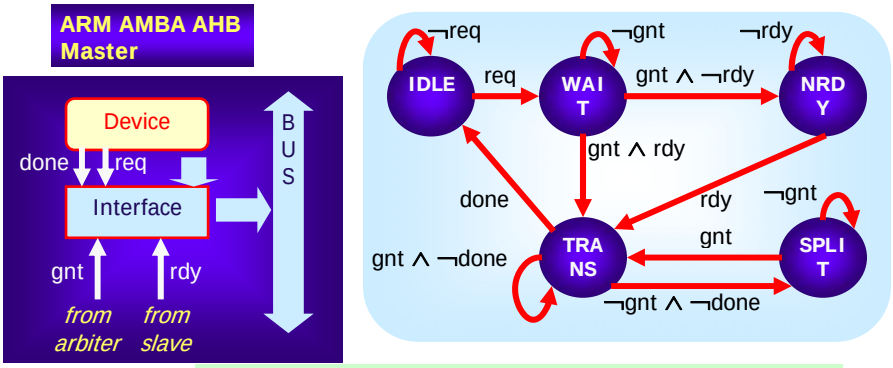
Model Checking Tools

The Formal-V group has expertise in designing both BDD-based and SAT-based model checking tools for formal property verification. Fundamental research by the group on the verification of assume-guarantee style properties on RTL modules has led to the development of the Open Family of Temporal Logics and an arsenal of model checking tools.



Is a granted master always able to transfer ?

In Open-CTL: AG(WAIT ⇒ AF_{gnt} TRANS) is false

Publications out of this work:

1. Banerjee, A., , Dasgupta, P., The Open Family of Temporal Logics, in ACM TODAES, 2005
2. Chakrabarti, A., Dasgupta, P., Chakrabarti, P.P., Banerjee, A., Formal Verification of Module Interfaces against Real Time Specifications, DAC 2002