Assertion Synthesis and Debug

In recent times, the Formal-V group is working on two key issues, namely, assertion synthesis and assertion debug. Assertion synthesis is primarily intended to provide the path to the designer to model undesirable conditions as assertions that will be synthesized as hardware blocks and fabricated on chip. Whenever an exception occurs, these on-chip exception handlers would take over and save the circuit from catastrophic disasters. In addition, some of the recent research of the Formal-V group has been in the area of Assertion Debug, whereby, the exact cause of assertion failure can be extracted and presented to a verification engineer for necessary action at a higher level of the design cycle.

Publications/Communications out of this work:

1. Nandi, A., Pal, B., Chhetan, N., Dasgupta, P., Chakrabarti, P.P., H-DBUG: A High-level Debugging Framework for Protocol Verification using Assertions. In Proceedings of INDICON, 2005.

2. Pal, B., Nandi, A., Dasgupta, P., Chakrabarti, P.P., H-DBUG: A Debugging Utility For Assertion-Based Protocol Verification, In Proc. of EAIT, 2006

3. Das, S., Dasgupta, P., Chakrabarti, P.P., Synthesis of SystemVerilog Assertions. In Proc. of DATE'2006, Munich, Germany, 2006.