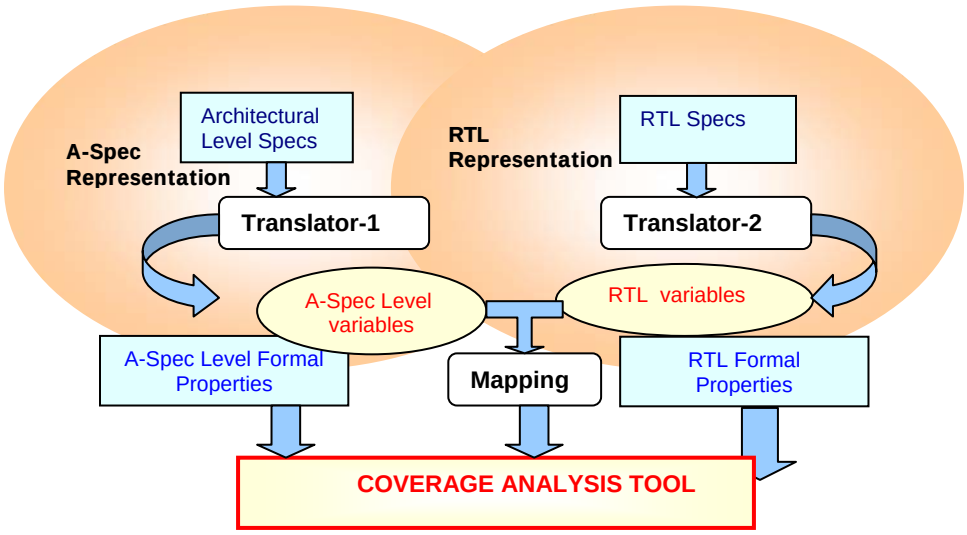
Design Intent Coverage

Current practice requires manual translation of a design's architectural intent into the RTL specifications of the component modules. This is widely recognized as one of the main sources of design errors. New technology developed by the Formal-V Group enables the design architect to express the intent in terms of formal properties and formally verify whether the RTL specification covers this intent. This helps in formalizing the completeness of the RTL specs prior to RTL implementation.



Publications out of this work:

1. Basu, P., Das, S., Banerjee, A., P. Dasgupta, Chakrabarti, P.P., Mohan, C.R., Fix, L., Armoni R., Design Intent Coverage – A new paradigm for Formal Property Verification, To Appear in IEEE TCAD

2. Das, S., Basu, P., Dasgupta, P., Chakrabarti, P. P., What lies between Design Intent Coverage and Model Checking? In Proc. of DATE 2006

3. Basu, P., Das, S., Dasgupta, P., Chakrabarti, P. P., Discovering the Input Assumptions in Specification Refinement Coverage, In Proceedings of ASPDAC 2006.

4. Basu, P., Dasgupta, P., Chakrabarti, P. P., Mohan, R. C., Property Refinement Techniques for Enhancing Coverage of Formal Property Verification, In Proc. of VLSI 2004.

5. Basu, P., Das, S., Dasgupta, P., Chakrabarti, P. P., Mohan, R. C., Fix, L., Formal Verification Coverage: Are the RTL-Properties Covering the Design's Architectural Intent?, In Proc. of DATE 2004