Formal Verification Research

Indian Institute of Technology Kharagpur

Formal-V Group, IIT KGP

The Formal-V research group at the Dept. of Computer Science & Engineering, Indian Institute of Technology Kharagpur offers exciting research opportunities in the emerging area of formal methods for design validation.

Highlights:

- **Ongoing projects with several companies, including Intel, Synopsys, National Semiconductors, General Motors and Interra EDA. Ongoing research projects with the Govt. of India, and academic institutions in other countries.**
- **More than 30 publications in leading journals and conferences in the last 3 years, including IEEE TCAD, ACM TODAES, DAC, ICCAD, ASPDAC, DATE and VLSI Design.**
- **State-of-the-art toolsets available at the Advanced VLSI Lab, IIT Kharagpur. This includes EDA tools from Cadence, Synopsys, Mentor.**

The family:

- **Mentors: Prof. P.P. Chakrabarti and Dr. Pallab Dasgupta**
- **8 PhD students**
- **More than 8 graduate students**

Benefits:

- **Exciting industrially relevant research problems**
- **High value fellowships**

For more information, visit our home:
http://www.facweb.iitkgp.ernet.in/~pallab/forverif.html

Computer Science, Electronics, and Electrical Engineering students with outstanding academic records may contact us (with resume) for open positions in ongoing and forthcoming projects.

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