ADVANCED VLSI DESIGN LABORATORY

Infrastructure for Excellence

Indian Institute of Technology Kharagpur, India
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ADVANCED VLSI DESIGN LAB
IIT KHARAGPUR

In the year 2000, the golden jubilee of IIT Kharagpur, the IIT Foundation came up with a visionary plan to set up a state-of-the-art VLSI Design Laboratory in its alma matter. Over the last seven years, this laboratory has achieved expertise to facilitate world class research in design, test and CAD. The Lab has established design and verification flows using standard EDA tools from Cadence, Synopsys, Mentor. In 2007, the Lab was able to procure state-of-the-art test equipment from a special grant provided by the institute.

A number of thrust areas have now emerged based on core competency available in the Institute. These include analog and RF circuits, wireless communication and Baseband processing, direct conversion receivers, power management circuits, processors and IP cores for embedded applications and design for testability. More than 60 different chips have been fabricated and tested. Apart from the large number of publications, students have also won regular awards in major design contests.

Faculty members have also taken up state-of-the-art collaborative research with many industries like National Semiconductors, Sun, Synopsys, Intel and IBM. The laboratory also offers regular intensive training to students of IIT Kharagpur on design and CAD. More recently, research directions are diversifying to new areas of mixed-signal SOCs, IP cores for embedded applications and analog DFT. Existing expertise on formal verification and optimization methods are being applied to design verification, synthesis and CAD for deep sub-micron processes.

In April 2006, the Lab launched the AVLSI Consortium comprising members from leading industry to support its high quality research activities. The consortium provides a forum for its members to share their ideas, mentor the research activities and share the research output. Today the consortium has about 15 member companies.

Currently more than fifty Doctoral and Masters students work under the ambit of the Lab on various emerging areas.

HIGHLIGHTS OF ACTIVITIES

- More than 30 publications in the last year
- More than 60 chips taped out from the laboratory
- Design of On-chip Single Inductor Triple Output DC-DC converter won the first prize in the Cadence Design Contest, 2007
- 15 leading companies have joined the AVLSI Consortium
- 11 ongoing projects under the AVLSI Consortium
- More than 12 ongoing collaborative research projects funded by the Govt. of India and leading companies including National Semiconductors, Intel, Synopsys, Infineon, Texas Instruments, Si2 Microsystems, Xaneda Technologies, Agilent, Tessolve, Analog Devices and General Motors

THRUST AREAS

The Advanced VLSI Lab has achieved core competence in various niche areas under the following broad headings:

- Analog and Mixed-signal Design, Verification & Test
- Digital Design, Verification & Test
- Behavioral Modeling and Architectural Exploration
- Wireless and RFIC
- Power Management Circuits
- Low power Design and Test
- MEMS and Nano-Electronics
- Biomedical, Telecommunication and Automotive applications
- Next Generation Integrated Devices

POWER MANAGEMENT GROUP

Portable power supplies are an integral part of most portable devices, including PDAs, Laptops, Automobiles and many more. The power management group in the Advanced VLSI Design Laboratory, IIT Kharagpur, has been very successful over the last 5 years in coming up with several very good designs. The research focus is broad targeting high power multiphase converters for laptop applications to very high frequency switchers, single inductor multiple output converters to EMI applications. Some areas of strength include:

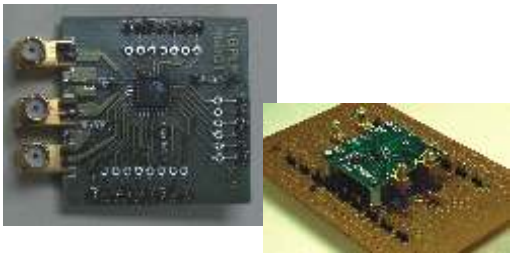
- High Frequency (20MHz) DC-DC converters
- Single-Inductor Multiple-Output DC-DC converter
- Multiphase VRM's for laptop applications
- Spread-spectrum EMI reduction in DC-DC converters
- Low-voltage Low-ripple on-chip hybrid DC-DC converters
- Current sensing techniques for very high frequency switchers
- Start-up circuits for very low input boost converters
- Battery Charger using solar cell.

Research output of this group has resulted in more than 50 publications in last five years in reputed international journals and conferences. One of the designs has also won the **Cadence Design Contest 2007.**

Collaborative research partners:
National Semiconductor, Texas Instruments, Infineon Technologies.

Team Leaders:
Amit Patra, Siddhartha Mukhopadhyay, Pradip Mandal, Debaprasad Kastha, Souvik Chattopadhyay

Contact: amit.patra@ieee.org



WIRELESS & RFIC GROUP

In view of the pressing market demands for power efficient wireless communication chips specially to achieve a cost effective low-power solution for portable systems, the RFIC group has been developing state-of-the-art RF front end design capabilities. The areas of research focus and strength include:

- Low-power Single-chip RF Transceivers for Narrowband, Multi-band and UWB applications
- RF front-end for DVB-H
- Frequency Synthesizers
- RF/Analog Design Optimization
- Broad-band behavioural-modeling of RF passive components and interconnects
- Miniaturized CPW for mm-wave applications in SOC
- RF MEMS

Research output of this group has resulted in about 30 publications in last three years in reputed international journals and conferences.

Collaborative research partners:
Industries: National Semiconductors, Texas Instruments, Si2 Microsystems, Xaneda Technologies, Agilent, Tessolve, Analog Devices. ***Universities:*** Univ. of Washington (Prof. Dave Allstot), Univ. of Utah (Prof. Richard Brown), Univ. of Twente (Prof. Bram Nauta), Univ. of California Irvine (Prof. Marc Madou)
Team Leader:
Tarun Kanti Bhattacharyya

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VLSI TEST GROUP

With the advancement of fabrication technology post-manufacturing test of VLSI circuits is facing new challenges. The test team members of Advanced VLSI Deign Laboratory have been working on various projects and novel approaches to circuit testing. Testing of the chips designed and fabricated in-house are carried out by this group. Design activities related to ATPG and DFT for both analog and digital chips have been taken up. Research in the areas of DFT compliant Analog and Digital chips with BIST capabilities have been undertaken. In addition, practical training of students in advanced electronic circuit testing has been carried out. Areas of strength include:

- On-Line Testing
- Behavioural Modeling for Concurrent Test Program Development
- Post-silicon Validation
- Design for Test and Test optimization
- Test support for in-house chip designs

Research output of this group has resulted in about 50 publications in last five years in reputed international journals and conferences.
Collaborative research partners:
National Semiconductors, Agilent Tech., Tesslove, Intel Corp.
Team Leaders:
Siddhartha Mukhopadhyay, Amit Patra

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HIGH PERFORMANCE DEVICE (SEMICONDUCTOR PROCESS) GROUP

The focus of this group is the realization of non-Silicon Integrated Circuits on Silicon substrate through novel metamorphic buffer epitaxial processes. Superior material characteristics & band gap engineering of compound semiconductors, as active layer material, lead to very low to very high voltage operation, high linearity, low noise, improved power output, and ultra high frequency of operation. Our potential solution is converged to the strategic integration of the superior properties of compound semiconductors with the matured technology of silicon; by sophisticated well developed crystal growth/process techniques like MBE/ MOCVD. More specifically, our journey paves to:

- High Indium content channel on metamorphic buffer HEMT/HBT for very high frequency low noise applications.
- Cubic Gallium Nitride based high linear, high power RF devices.
- Gallium Nitride based optical devices.

Our collaborative framework will complete the technology ecosystem (RFIC/MMIC empowered systems for energy, environment, agro-industrial, security and health-care sectors) which will help to transform India into a sustainable knowledge economy.
Team Leader:
Dhrubes Biswas

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DIGITAL DESIGN GROUP

The digital design group of Advanced VLSI Design Lab aims at enhancing the computational power to boost the efficiency of digital circuits while reducing the power consumption and the area requirement. Team members are involved in research activities that foster novel approaches to various problems encountered by the digital world. Areas of strength include:

- Digital Design Methodology
- ASIC design
- Implementation of various DSP algorithms in Hardware
- Low power architecture
- Fault tolerant architecture
- Real time systems designing
- High speed system design
- System prototyping using FPGA

Various research publications in leading journals and conferences along with prizes from design contests show the excellence of this team is well appreciated. Some of the recent products from this group include:

- Cryptography Processor design
- Base band processor design for UWB communication
- Efficient realization of ASR system
- ASIC for Real Time Image registration
- CORDIC based VLSI Architecture Design

Team Leaders:
A. S. Dhar, S.Chakrabarti, G. Saha

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MEMS & SIGNAL CONDITIONING GROUP

Micro-electro-mechanical systems, or MEMS, is an emerging area with applications in a variety of engineering fields such as aerospace, mechanical, electrical, communications etc. It was the automotive industry which first commercially embraced MEMS devices as airbag accelerometers, recognizing the benefits of MEMS devices' small size, relative low cost and high degree of sensitivity. Today, because of MEMS, the accelerometer and electronics are integrated on a single chip at a cost of under $10. This group is mainly working on a project to design and fabricate a surface micro-machined MEMS structure for capacitive accelerometer suitable for automotive applications and its corresponding signal conditioning circuit. Some of the key features are:

- Surface Micro-machined MEMS.
- Inter-digitized comb shaped structure, variable gap type.
- Over range protection, self structure, etch hole over proof mass incorporated.
- ASIC capable of detecting capacitance variation ~ fF.
- Fully OTA based design including Gm based amplifiers and filter.
  Hybrid integration of MEMS and ASIC.

Collaborative research partners:
DIT, Govt. of India, SCL, Chandigarh.
Team Leaders:
Siddhartha Sen, Amit Patra.

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ANALOG AND MIXED-SIGNAL GROUP

The field of Analog and Mixed-signal design is an indispensable part of integrated circuit design in modern era on account of the fact that the need is to integrate complete systems, rather than mere sub-systems, are on a single chip (SOCs). Therefore the activities of this group are focused on the

design and fabrication of state-of-the-art integrated circuits in the Analog and Mixed-Signal domain. The research is primarily focused on the following:

- A/D Converters: High-Precision Sigma Delta ADC and High-Speed ADC
- High-Performance & Low Power Analog Building Blocks: High-speed Operational Amplifier, Advanced analog computation circuits for neural networks and Low jitter Multiphase Clock Generator
- Analog Circuit Modeling: Operational Amplifier Macro modeling

Research output of this group has resulted in about 30 publications in last five years in reputed international journals and conferences.

Collaborative research partners:
National Semiconductors, Analog Device, Si2micro

Team Leaders:
Prof. Amit Patra, Dr. T.K. Bhattacharyya, Dr Pradip Mandal, Prof. N. B. Chakrabarty, Prof. Goutam Saha

International Collaborators

- Dr S.E.Ralph, Georgia Institute of Technology, Atlanta, USA
- Dr K.Pedrotti, University of California, Santa Cruz, USA
- Dr E. Klumperink, Prof. B. Nauta, University of Twente, Netherlands
- Prof. Franco Maloberti, University of Pavia, Italy

Contact: amit.patra@ieee.org

VERIFICATION AND CAD GROUP

Verification is a major problem in all types of engineering design. The formal verification research group focuses on providing industrially relevant formal methods for the verification of various designs ranging from digital and mixed-signal chip designs to complex software and embedded systems such as automotive control systems. Areas of strength include:

- Design Intent Verification
- Formal Verification Coverage
- Mixed-signal Design Verification
- Coverage-driven Semi-Formal Verif.
- Verification of Automotive Systems
- Verification of Web Interfaces

Research output of this group has been recognized world-wide in terms of research publications in leading journals and conferences, courses and tutorials delivered world-wide, and productization of technology by industry partners.

Collaborative research partners:
Intel, Synopsys, General Motors, National Semiconductors, Google, IBM, Sun Microsystems and Interra Systems.

Team Leaders:
Pallab Dasgupta, P.P. Chakrabarti, D. Sarkar

Home: http://www.facweb.iitkgp.ernet.in/~pallab/forverif.html

Contact: pallab@cse.iitkgp.ernet.in

OPPORTUNITIES

If you are a student or aspiring to be one:

1. Join as a regular MS/PhD student at IIT Kharagpur with attractive remunerations from the AVLSI Lab.
2. Sponsored part time students: One semester course work at IIT Kharagpur and research at your industry.

If you are a working professional with aspirations of collaborative research with us:

1. Your company may join the consortium and participate in shaping / mentoring the research in the Lab with your leadership.
2. Directly funded collaborative research projects with the Lab in areas of mutual interest.

If you are an expert in your area from the industry or the academia:

1. Please do visit us and advise us in shaping our roadmap.
2. You may also consider participating in the lab activities as an adjunct faculty member.

FACULTY

- *Ajit Pal, Computer Science & Engineering*
  Low Power Design, CAD for VLSI, Embedded Systems
- *Alok Barua, Electrical Engineering*
  Analog Signal Processing, Artificial Intelligence, Bio-reactor Control & Instrumentation
- *Amit Patra, Electrical Engineering*
  Power Management Circuits, Analog and Mixed-Signal Design and Test, Behavioral Modeling
- *Anindya Sundar Dhar, Electronics & Electrical Communication Engineering*
  VLSI Design
- *Chandan Chakraborty, Electrical Engineering*
  Electric Vehicles, Electrical Machines and drives, Power electronics, Non conventional energies
- *Chittaranjan Mandal, Information Technology*
  VLSI Design, Formal Verification, High level Synthesis, Algorithms, Computer Vision
- *Debasis Samanta, Information Technology*
  VLSI Design, Human Computer Interaction, Object Oriented Design
- *Dhrubes Biswas, Electronics & Electrical Communication Engineering*
  Semiconductor Processing
- *Dipankar Sarkar, Computer Science & Engineering*
  Formal Verification, Embedded Systems, CAD for VLSI
- *Dipanwita Roy Choudhury, Computer Science & Engineering*
  Cellular Automata, VLSI Design and Test, Cryptography
- *Goutam Saha, Electronics & Electrical Communication Engineering*
  Biomedical signal processing, Speech processing
- *Indrajit Chakrabarti, Electronics & Electrical Communication*
  VLSI Design
- *Indranil Sengupta, Computer Science & Engineering*
  VLSI Design and Testing, Cryptography
- *Jayanta Mukhopadhyay, Computer Science & Engineering*
  Image Processing, Multimedia Systems
- *Mrityunjoy Chakraborty, Electronics & Electrical Communication*
  Digital and Adaptive Signal Processing, VLSI Signal Processing
- *N B Chakraborty, Sponsored Research & Industrial Consultancy*
  VLSI Design
- *Niloy Ganguly, Computer Science & Engineering*
  Peer-to-peer Networks, Network Theory, VLSI Test and Design
- *Pallab Dasgupta, Computer Science & Engineering*
  Formal Verification, CAD for VLSI
- *Partha Pratim Chakrabarti, Computer Science & Engineering*
  CAD for VLSI, Algorithms, Formal Verification
- *Prabir Kumar Biswas, Electronics & Electrical Communication*
  Computer Vision, Fuzzy and Neural Computing
- *Pradip Mandal, Electronics & Electrical Communication*
  Analog VLSI Design, CAD for VLSI

- *Rajeev Kumar, Computer Science & Engineering*
  Genetic Optimization, Multimedia, Programming Languages
- *Ratnam Varada Rajakumar, Electronics & Electrical Communication*
  Wireless Networks, Digital Signal Processing
- *Santanu Chattopadhyay, Electronics & Electrical Communication*
  Logic Synthesis, Cellular Automata, Circuit Testing, Low Power Design and Test, System-on-Chip Testing
- *Santiram Kal, Electronics & Electrical Communication*
  ASIC, IC Technology, MEMS, Microsensors & Microsystems, Microelectronics, VLSI Design, Thin Films
- *Saswat Chakrabarti, G S Sanyal School of Telecommunications*
  Wireless Communications, Error Control Coding, Digital Modulation Schemes, Mobile Adhoc Networks, Bio-telemetry
- *Shamik Sural, Information Technology*
  VLSI Design, Document Analysis, Computer Vision, Multimedia Databases, Pattern Recognition
- *Siddhartha Mukhopadhyay, Electrical Engineering*
  Discrete Event Systems, Embedded systems, Fault Detection and Diagnosis, Industrial Automation, Instrumentation and Control
- *Sidhartha Sen, Electrical Engineering*
  Capacitive sensors, Electrical Impedance Tomographic Imaging, Fault Tolerant Control, Robust Control
- *Soumya Kanti Ghosh, Information Technology*
  Multimedia
- *Souvik Chattopadhyay, Electrical Engineering*
  VLSI Design
- *Tarun Kanti Bhattacharyya, Electronics & Electrical Communication*
  MEMS, Microelectronics, Thin films, VLSI Design

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