STATEMENT OF PURPOSE

"Stay hungry, stay foolish"

Steve Jobs
[Commencement Address, Stanford University, 2005]

I first felt the thrill of pursuing a dedicated scientific research, when I read about Prof. Andrew Wiles, (who spent seven years in isolation, solving the toughest riddle of mathematics) in the popular book - ``*The Fermat's Last Theorem*" by Simon Singh, in my sophomore undergraduate year. Since then, the passion to *excel* and to *innovate*, has always hosted a *hungry* and *foolish* soul in me. My primary research interests are in the fields of CAD for VLSI, Computer Architecture and Formal Verification.

My Academic and Research Background
Smart problem-solving has always been a source of great fun to me. Mathematics was my favorite subject in school. As a token of appreciation for my hobby activities in mathematics, I was awarded **C. V. Raman scholarship** during my high-school days at *Ramkrishna Mission Vidyalaya, Narendrapur*. My confidence was further boosted when I stood 4th in the **Regional Mathematical Olympiad** in 2001 and was selected to participate in **Indian National Mathematical Olympiad (INMO)**.

It was a great opportunity to study at the **Indian Institute of Technology, Kharagpur**, one of the premier engineering institutes in India, in my desired discipline of *Computer Science & Engineering*. Ever since I joined the department, I have been focused on my academics which culminated in my high CGPA (**9.28/10.00**), and a rank of **First** in the department (out of 23 students) and **Fifth** in the institute (out of approximate 200 students).

My first brush with VLSI was in the summer (May-June) of 2004, when I was selected for a month-long training at the **Advanced VLSI Design Laboratory, IIT Kharagpur**. I came to know about the challenges of design and verification of complex digital as well as analog VLSI circuits and got exposed to the various CAD tools. In the following paragraphs I list my major research endeavors that shaped my interest.

Summer Internship 2005*:* I did my summer internship under **Prof. Rainer Leupers** at the **Institute for Integrated Signal Processing (ISS), RWTH, Aachen, Germany**. I integrated a semi-formal (assertion-based) verification approach for processors designed in **Language for Instruction Set Architecture (LISA)** and also developed an automatic test-pattern generator from the ADL description. Moreover, I understood that how the international composition of a research group helps in carrying out effective research. Our work resulted in the following paper
Anupam Chattopadhyay, Arnab Sinha, Diandian Zhang, Rainer Leupers, Gerd Ascheid, Heinrich Meyr, ``*Integrated Verification Approach during ADL-Driven Processor Design*" rsp, pp. 110-118 in **17th IEEE International Workshop on Rapid System Prototyping (RSP'06), 2006** held in **Crete, Greece**.

B.Tech Project*:* In my Senior Year, I worked on a project funded by **Synopsys Inc.** with **Prof. P. P. Chakrabarti** and **Dr. Pallab Dasgupta** as its principal investigators. The project had two distinct parts to it. First, it is to synthesize a given set of linear constraints into hardware with a non-backtracking algorithm. A paper ``*Hardware Accelerated Constrained Random Test Generation*" based on this work has been communicated to IEEE Design & Test. Second, we addressed the following question, ``*Can we extract the relevant assumptions from a well structured constrained random test bench?*" This project named, ``**Synthesis and Model Extraction of A Constrained Random Test-bench**" was nominated for the **Best B.Tech Project** in the department.

Summer Internship 2006*:* Impressed with my previous performance, Prof. Rainer Leupers invited me once again for an internship in Aachen in May-July 2006. In this project, we have proposed a novel backtracking algorithm for cycle-accurate pipelined processors to obtain the test-pattern, targeting the coverage of each conditional block of the processor description. A paper, ``*ADL-driven Automatic Test Pattern Generation for Functional Verification of Embedded Processors*, has been submitted to 12th IEEE European Test Symposium (**ETS, 2007)**.

Arnab Sinha / September 22, 1983 / Applying to PhD, Department of Electrical Engineering, Princeton U.

***Current Research Activities**:* Recently, I have worked with automatic test generation algorithm for designs where the properties are written on internal micro-architectural events which are absent in the interface between DUT and test bench. A paper on this work: "*Property driven Intelligent Test Generation In Absence of Direct Interface*", has been communicated to Great Lakes Symposium on VLSI (**GLSVLSI, 2007**).

I am currently working on design intent coverage problem of the architectural state-machine based specifications. Here the properties are written on the abstract state-machine based model. Although this style helps in expressing properties in a better way, the fictitious model in the block-level specifications adds to the challenge of the verification engineer.

During my active involvement in these projects, I developed a keen interest in Architectures of Computer and Application Specific Instruction-Set Processor (ASIP), Formal Specification and Verification, CAD for VLSI and Architecture Description Languages (ADLs). My experience in CAD and verification made me realize the expanding demand for more sophisticated and scalable architecture and CAD tools. Hence, I have decided to pursue graduate studies in order to gain deeper insight into these areas.

My Extra-curricular Interests:
Besides academic interests, I am also fairly active in literary activities (remained **Captain** in Bengali Literary Activities in my hostel for last two years and have led my hall in accomplishing several accolades), dramatics, and debating (stood **First** in **All India Debate Competition** organized by **National Council for Education Research and Training (NCERT)**). Besides, I have a strong acumen in strategizing. (Won **3rd** position in a Marketing Consultancy Competition called *Case-a-Franca*). Moreover, I was the member of the Problem Design Team in **Bitwise**, 2006, *Algorithm Intensive Programming Contest* organized by Dept. of Computer Science and Engineering, IIT Kharagpur.

My Aim:
As an Indian student of technology, my primary focus is to develop something which is low-cost, fitting to our national mindset and targeted to serve Indian necessities, e.g projects like *Shruti* and *Sanyog* in IIT Kharagpur are worth mentioning in this context. I enjoy doing independent research. Moreover, I have been teaching assistant to two courses (Operating Systems and Advances in Algorithms). In this way, I have discovered my flair for teaching too. After the doctoral studies I visualize myself as a productive researcher as well as an active faculty member.

Why Princeton?
I wish to be in a place, where I can learn, how to incubate an elegant idea, formulate it succinctly and passionately strive to reach the goal with scientific integrity. During my undergraduate studies, I came across numerous examples of great ideas developed at Princeton (e.g. ZChaff). I have gone through the research interests of the faculty and I am excited to find that my area of focus has been well represented through the ongoing projects. Moreover, I have personally communicated with Prof. Niraj K. Jha and Prof. Sharad Mallik, whose research topics seem to match my interests well. All these factors made Princeton a natural choice for me. I sincerely believe that with my hard work and dedication I will be able to live up to the high standards expected of a graduate student at the Princeton University.

Arnab Sinha