Error Detection - 02.03.2006

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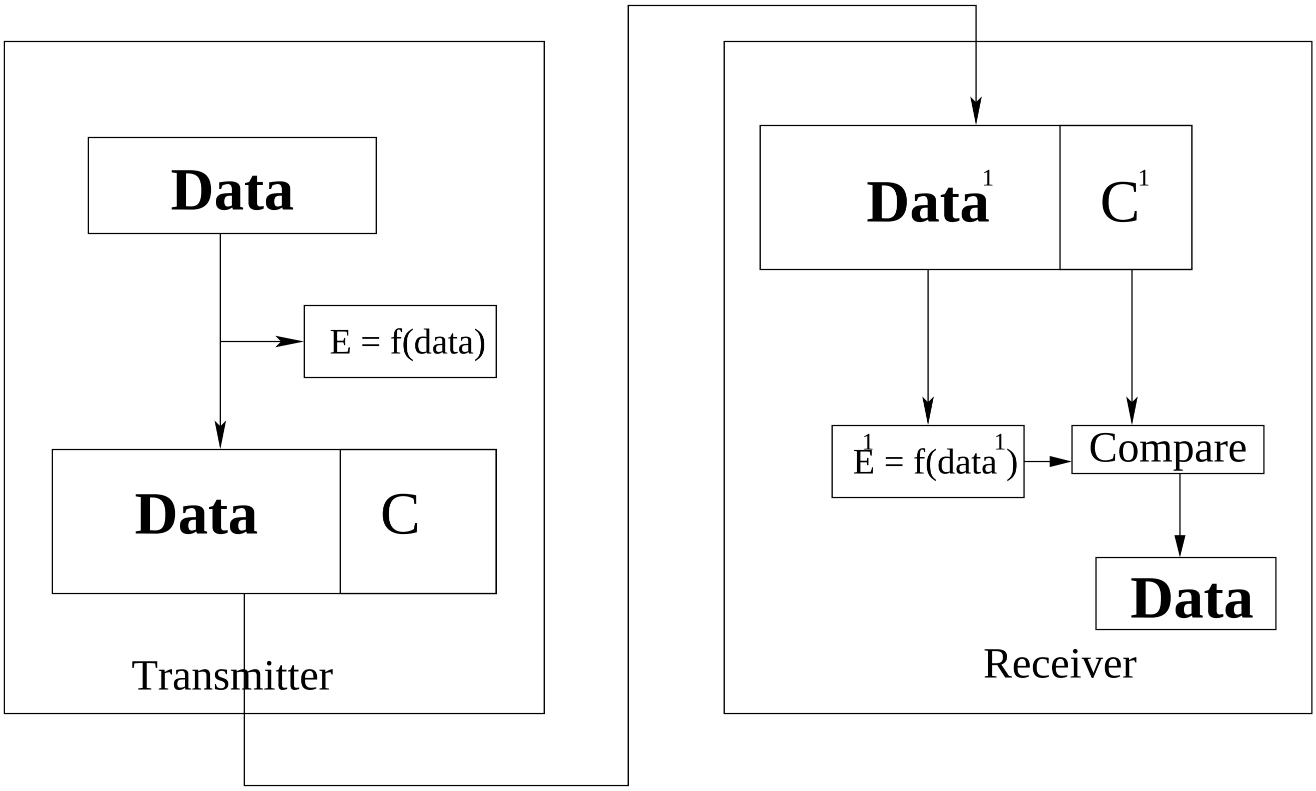
[1]Ref: Data and Computer Communications by William Stallings

Error Detection

Regardless of the design of the transmission system, there will be errors, resulting in the change of one or more bits in a transmitted frame. Also, the probablity that a frame arrives with no errors decreases with increasing frame length; the longer the frame, the more bits it has and the higher the probablity that one of these is in error.



For a given frame of bits,additional bits that constitute an error-detecting code are added by the transmitter. The code is calculated as a function of the other transmitted bits. For a data block of k bits, the error-detection algorithm yields an error detection code of n-k bits,where (n - k) is less than k. The receiver seperates the incoming frame into the k bits of data and (n - k) bits

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of error-detection code. The receiver performs the same error-detection calculation on the data bits and compares this value with th value of the incoming error detection code. A detected error occurs if and only if there is a mismatch.

Parity Check

The simplest error-detection scheme is to append a parity bit to the end of a block of data. A typical example is character transmission, in which a parity bit is attached to each 7-bit IRA character. The value of this bit is selected so that the character has an even number of 1s (even parity) or an odd number of 1s (odd parity).

Note,however,that if two (or any even number) of bits are inverted due to error, an undetected error occurs. The use of the parity bit is not foolproof, as noise impulses are often long enough to destroy more than one bit, particularly at high data rates.

Cyclic Redundancy Check (CRC)

Cyclic Redundancy check (CRC), is one of the most common, and one of the most powerful, error-detecting codes, which can be described as follows. Given a k-bit block of bits, or message, the transmitter generates an (n - k)-bit sequence, known as a frame check sequence(FCS), such that the resulting frame, consisting of n-bits, is exactly divisible by some predetermined number. The receiver then divides the incoming frame by that number and, if there is no remainder, assumes there was no error.

Define: T = n-bit frame to be transmitted

D = k-bit block of data, or message, the first k-bits of T

F = (n - k)-bit FCS, the last (n - k) bits of T

P = pattern of n - k + 1 bits; this is the predetermined dividor

We would like T/P to have no remainder. IT should be clear that

$$T = 2^{(n-k)} + F$$

That is, by multiplying D by $2\hat{(}$n - k), we have in effect shifted it to the left by n - k bits and padded out the result with zeroes. Adding F yields the concatenation of D and F, which is T. We want T to be exactly divisible by P.

The pattern P is chosen to be one bit longer than the desired FCS, and the exact bit pattern chosen depends on the type of errors expected. At minimum, both the high- and low- order bits of P must be 1.

Example to explain it is given below:

Example: P = 110101

D = 101001101

```
110101 ) 10100110100000
         110101
         ------
          111001
          110101
          ------
            110001
            110101
            ------
              100000
              110101
              ------
               101010
               110101
               ------
                111110
                110101
                ------
                  01011
```

F = 01011