VLSI System Design

Assignment 1

Date of submission: August 10, 2018

Model the following problems in SPICE ***using netlist specification*** and carry out the analyses as specified. Make relevant assumptions where necessary.

All the assignments have to be submitted electronically as a single zip file with name **`<group no>-assign1.zip`**, and must contain relevant output files and plots with documentation where required. The file must be mailed to isg@iitkgp.ac.in, with copies to sayandeep.sanyal@gmail.com and brojogopal.sapui@gmail.com .

1. Create a circuit consisting of a chain of 2 nMOS pass transistors, with the gates of all the transistors connected to V_{dd}. Connect an nMOS inverter of suitable size at the output. Apply a pulse waveform at the input and observe the voltage degradation at the input of the inverter and also the corresponding delay.

   Repeat the simulation for 4, 6, and 8 pass transistors.

2. Repeat the above simulation experiment, replacing the nMOS pass transistors by transmission gates and using a CMOS inverter instead of nMOS inverter.

3. Consider a CMOS inverter. Carry out transient analysis and estimate the rise time and fall time delays, and also the current drawn from the power supply.

4. Consider a chain of two nMOS inverters with 4:1 geometry. Estimate the rise time and fall time at the outputs of the inverters, and hence the inverter pair delay.

   Also analyze the current drawn from the power supply, and the power consumption.

5. Model a 3-input NAND and a 3-input NOR using both nMOS and CMOS technologies, and analyze the performances in terms of delay, current drawn from the power supply, and the power consumption.