Practice Problems on Logic Simulation

1. For the circuit shown in Figure 1, perform event driven simulation for the three test vectors as shown. Assume that the AND, OR, NOT and NAND gates have delays of 3, 4, 1 and units, respectively. Summarize the result of simulation as a timing diagram.
2. For the circuit shown in Figure 1, perform parallel fault simulation using the three test vectors have mentioned. Hence explain how the same can be implemented in a compiled code simulation environment.

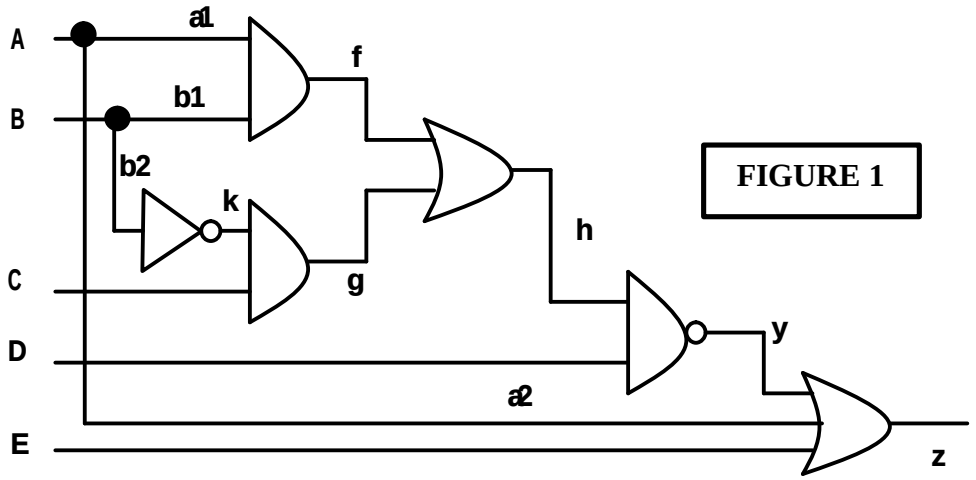

FIGURE 1

Test vector 1: A=0, B=0, C=1, D=1, E=0

Test vector 2: A=0, B=1, C=1, D=1, E=0

Test vector 3: A=1, B=1, C=0, D=1, E=0