IEEE 1149.1 JTAG
Boundary Scan Standard

Purpose of Standard

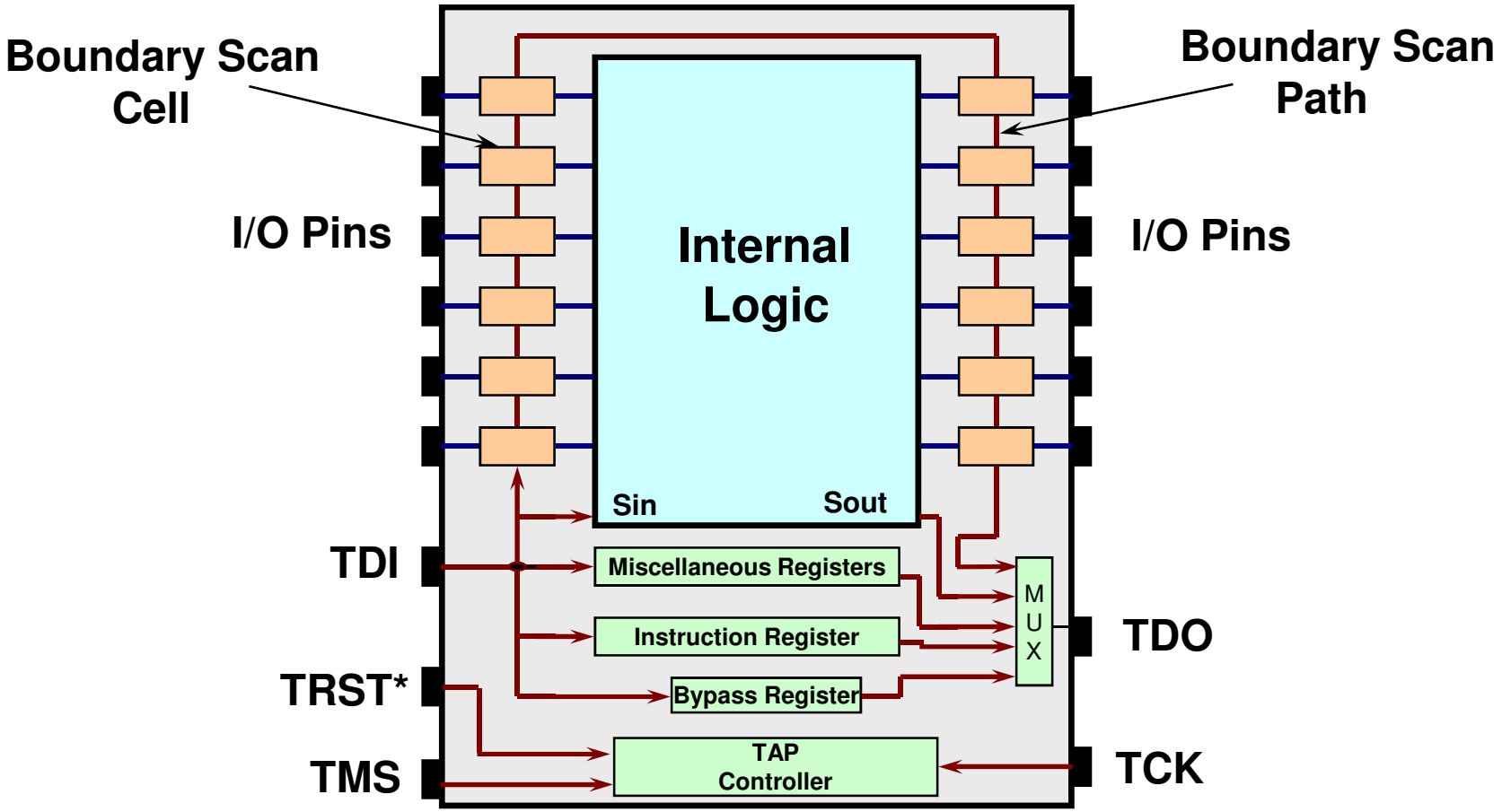
- Allow test instructions and test data to be serially fed into a component-under-test (CUT).
  - Allows reading out of test results.
  - Allows RUNBIST command as an instruction.
- JTAG can operate at chip, PCB, & system levels.
- Allows control of tri-state signals during testing.
- Allows other chips collect responses from CUT.
- Allows system interconnects be tested separately from components.

History

- 1985
  - Joint European Test Action Group (JETAG, Philips)
- 1986
  - VHSIC Element-Test & Maintenance (ETM) bus standard (IBM et al.)
  - VHSIC Test & Maintenance (TM) Bus structure (IBM et al.)
- 1988
  - Joint Test Action Group (JTAG) proposed Boundary Scan Standard
- 1990
  - Boundary Scan approved as IEEE Std. 1149.1-1990
  - Boundary Scan Description Language (BSDL) proposed by HP

- **1993**
  - **1149.1a-1993 approved to replace 1149.1-1990**
- **1994**
  - **1149.1b BSDL approved**
- **1995**
  - **1149.5 (Module Test and Maintenance Bus) approved**

Basic Chip Architecture for 1149.1

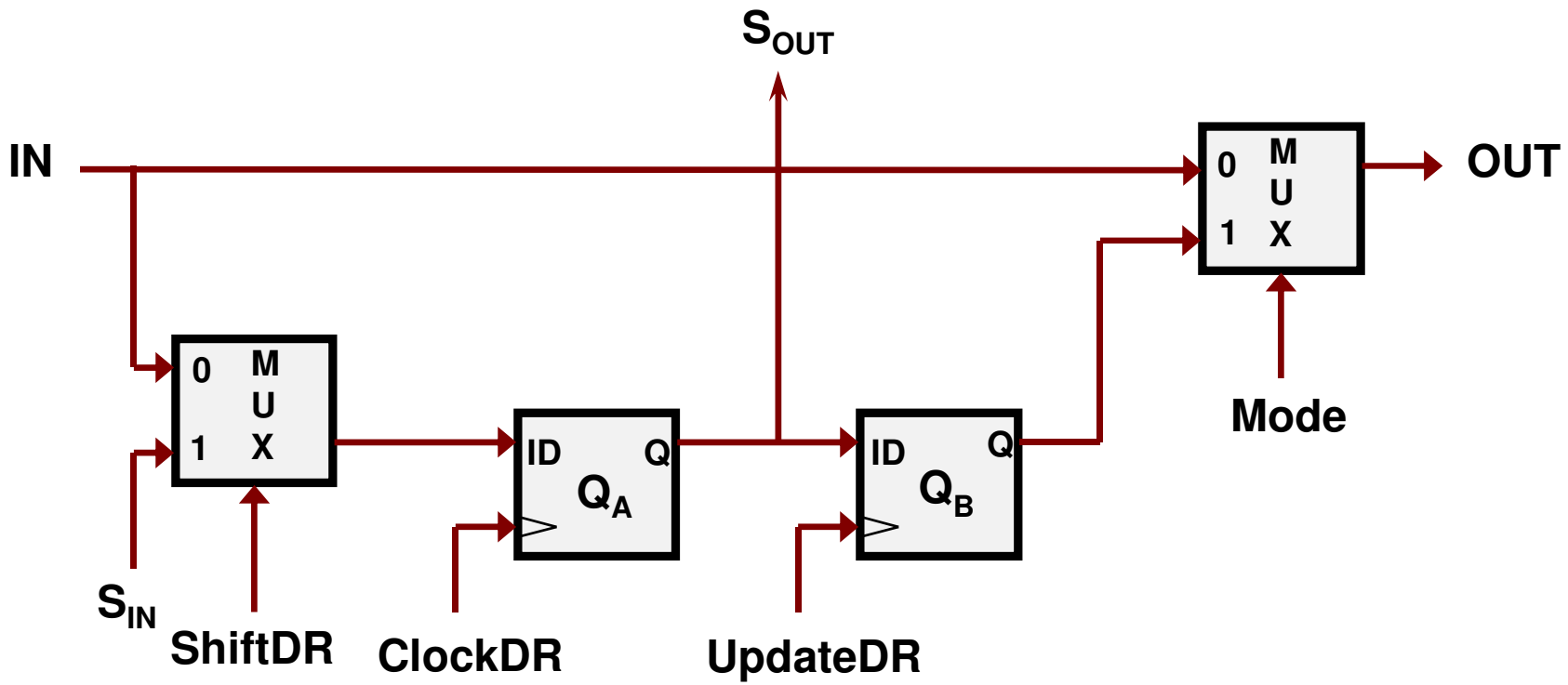


- Test Access Port (TAP)
- TAP controller
  - A finite-state machine with 16 states.
- Test Data Registers
  - Mandatory
    - Boundary scan register
    - Bypass register
    - Instruction register
  - Optional
    - Device-id register
    - Design-specific registers

- **Signals:**
  - **TDI:** **Test Data In**
  - **TDO:** **Test Data Out**
  - **TMS:** **Test Mode Selection**
  - **TCK:** **Test Clock**
  - **TRST* (optional):** **Test Reset**

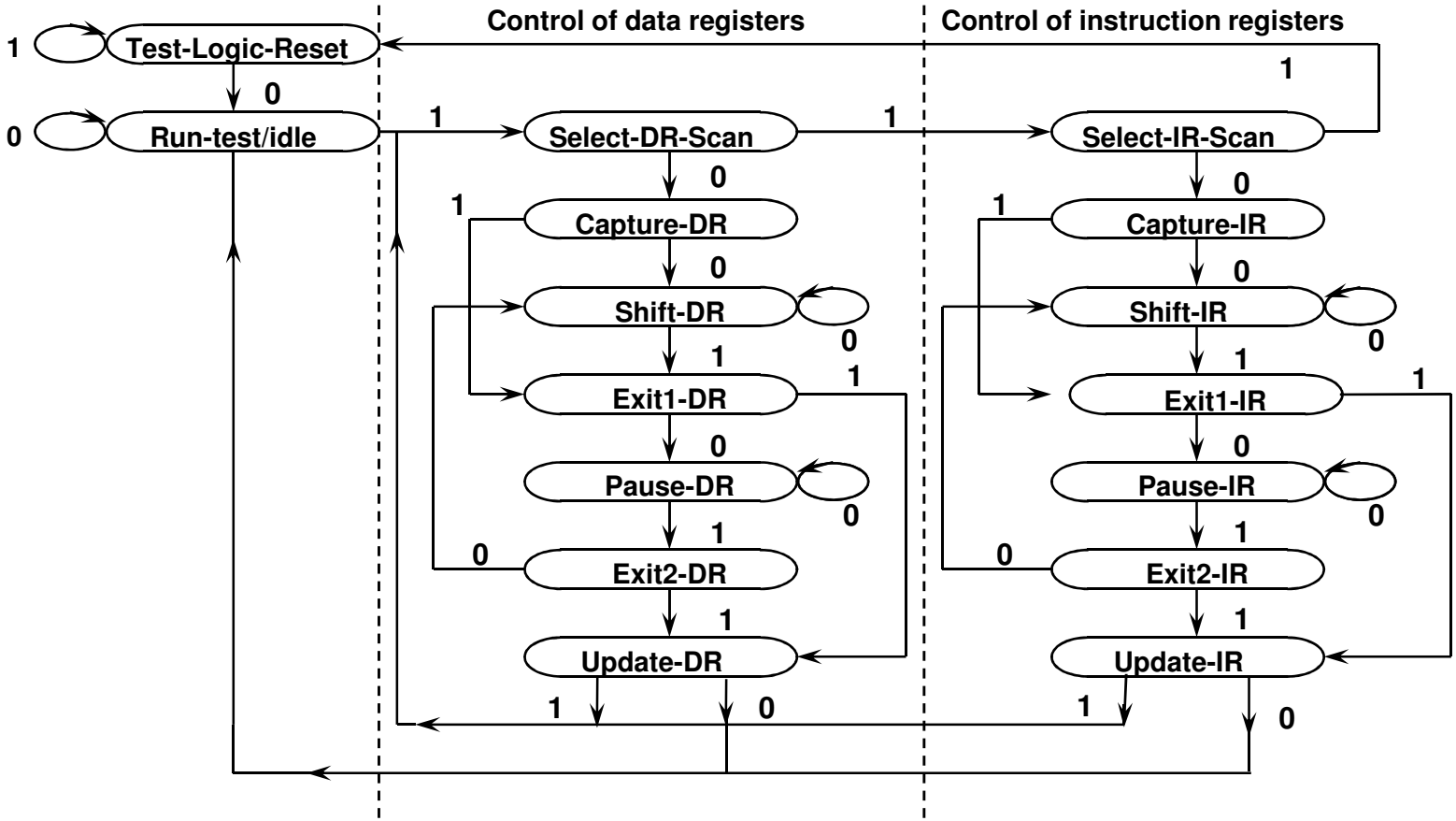
- **Basic operation:**
  - Instruction sent (serially) over TDI into instruction register.
  - Selected test circuitry configured to respond to instruction.
  - Test instruction executed.
  - Test results shifted out through TDO.
    - New test data on TDI may be shifted in at the same time.

Elementary Boundary Scan Cell



- **Operation modes:**
  - **Normal:** Mode = 0;
    IN $\rightarrow$ OUT
  - **Scan:** ShiftDR = 1, ClockDR;
    TDI $\rightarrow$ ... $\rightarrow$ S_{IN} $\rightarrow$ S_{OUT} $\rightarrow$ ... $\rightarrow$ TDO
  - **Capture:** ShiftDR = 0, ClcokDR;
    IN $\rightarrow$ Q_A, OUT driven by IN or Q_B
  - **Update:** Mode = 1, UpdateDR;
    Q_A $\rightarrow$ OUT

State Diagram of TAP Controller



States of TAP Controller

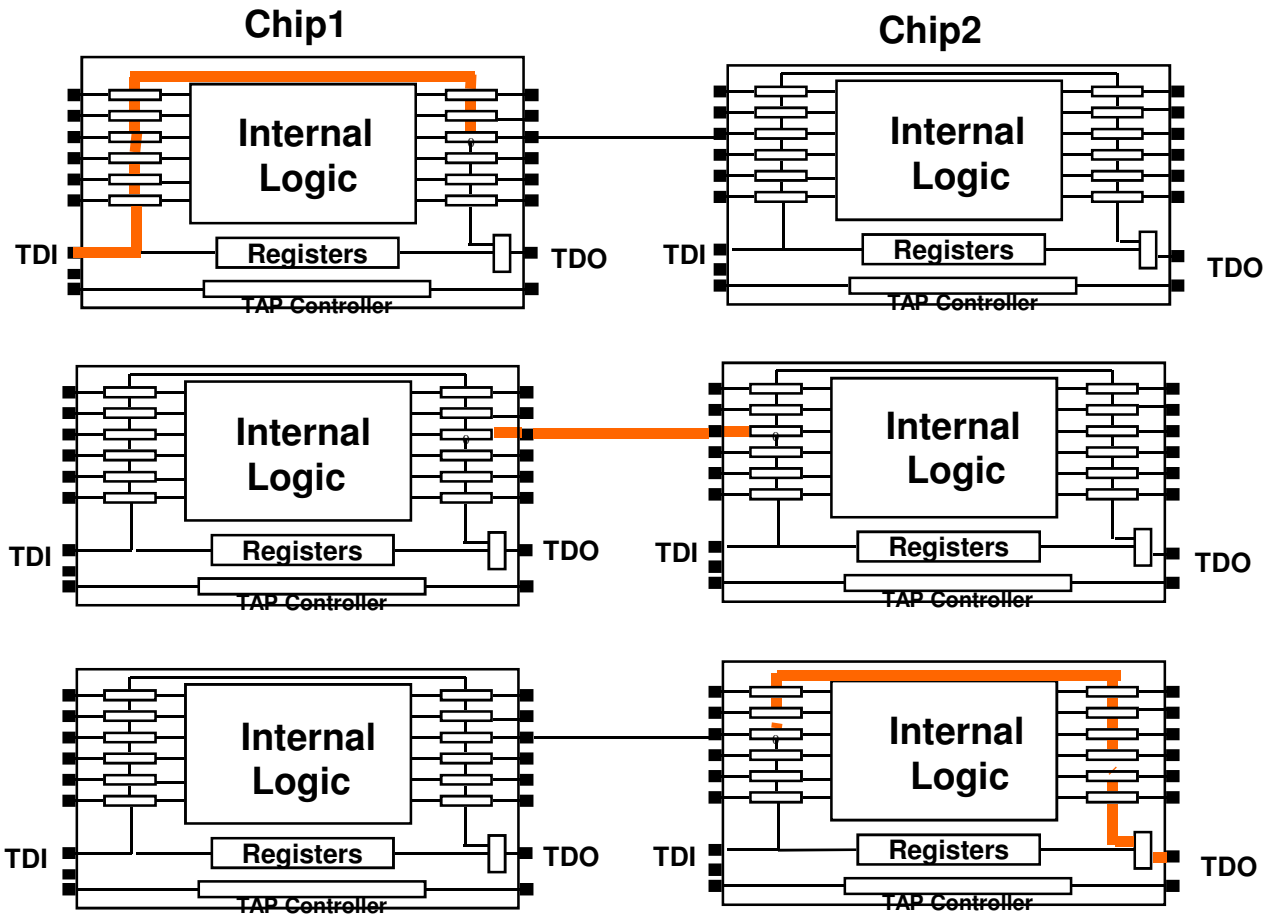
- **Test-Logic-Reset: normal mode**
- **Run-Test/Idle: wait for internal test such as BIST**
- **Select-DR-Scan: initiate a data-scan sequence**
- **Capture-DR: load test data in parallel**
- **Shift-DR: load test data in series**
- **Exit1-DR: finish phase-1 shifting of data**
- **Pause-DR: temporarily hold the scan operation (allow the bus master to reload data)**
- **Exit2-DR: finish phase-2 shifting of data**
- **Update-DR: parallel load from associated shift registers**

Instruction Set

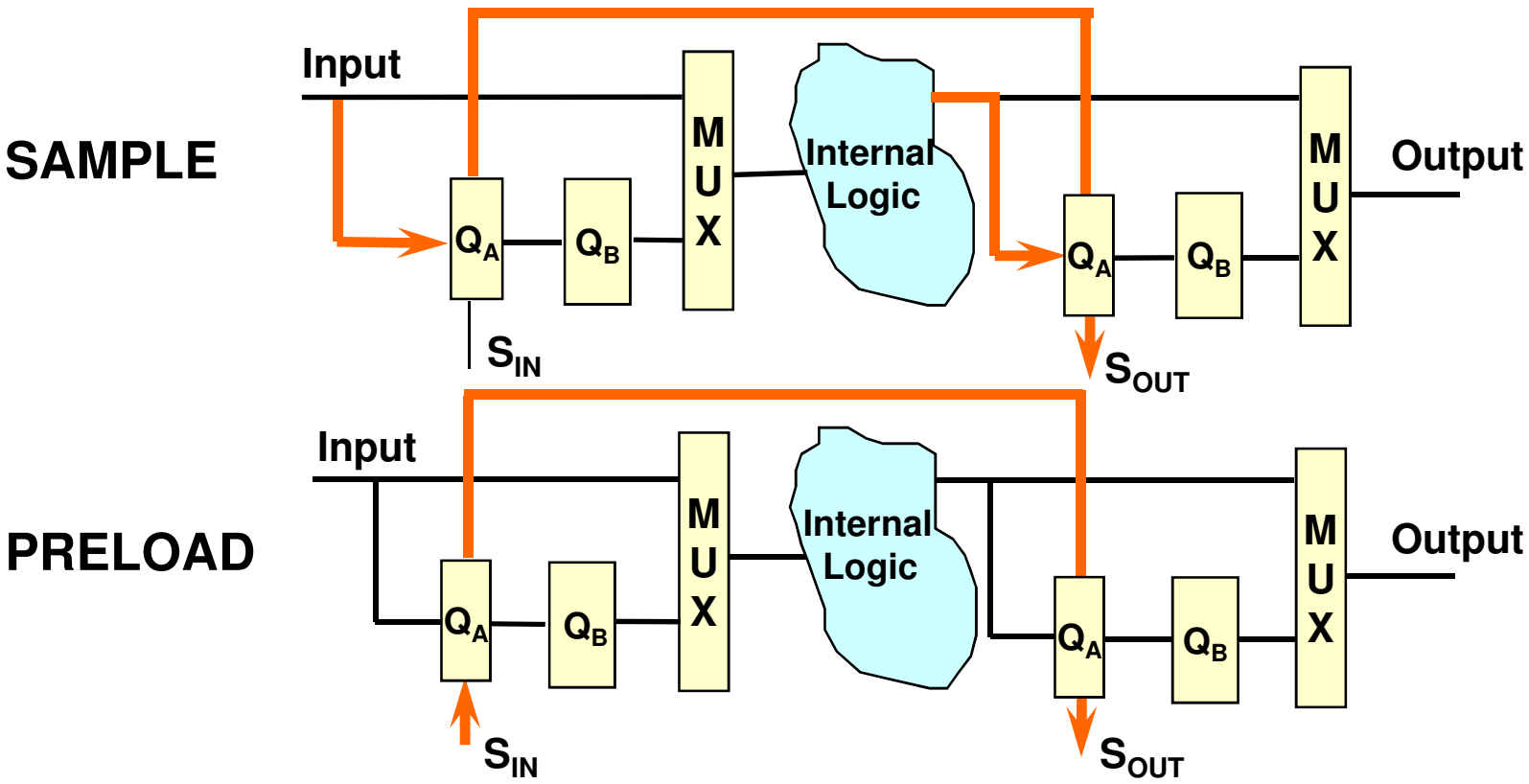
- **EXTEST**
  - **Test interconnection between chips on board.**
- **SAMPLE/PRELOAD**
  - **Sample and shift out data, or shift in data only.**
- **BYPASS**
  - **Bypass data through a chip.**
- **Optional instructions**
  - **INTEST, RUNBIST, CLAMP, IDCODE, HIGH-Z, USERCODE.**

EXTEST

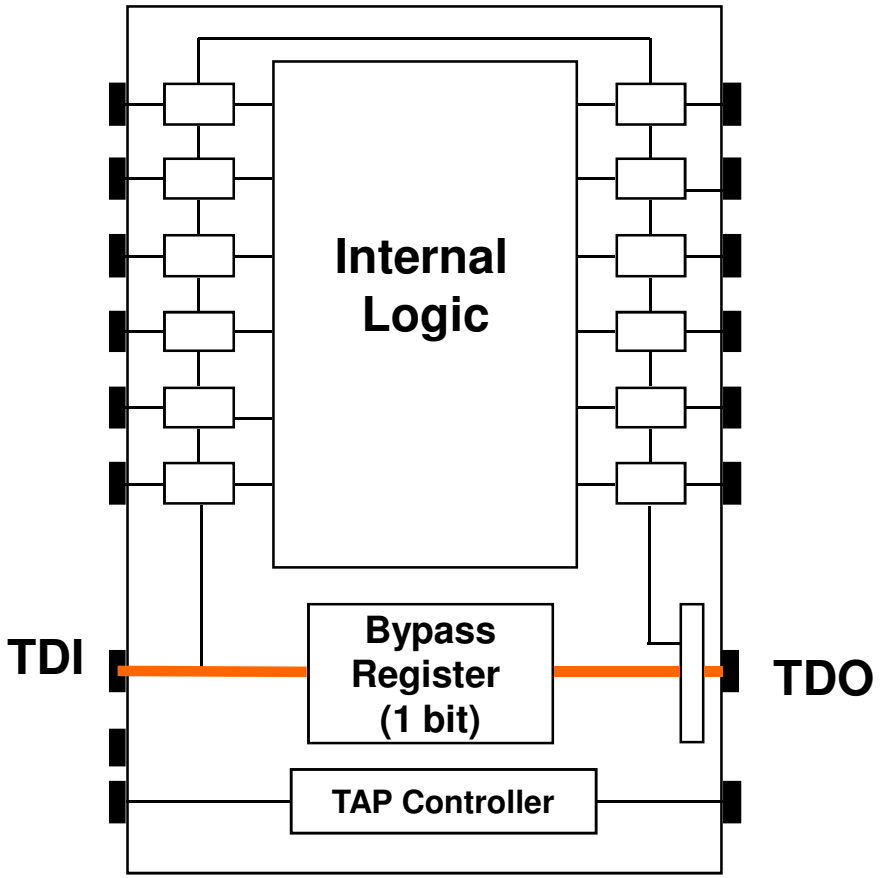
1. Shift-DR (Chip1)
2. Update-DR (Chip1)
3. Capture-DR (Chip2)
4. Shift-DR (Chip2)



SAMPLE/PRELOAD

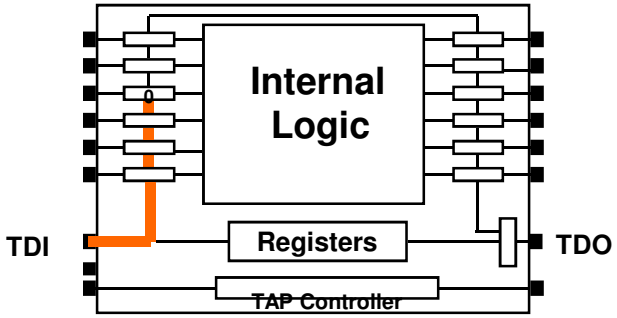


BYPASS

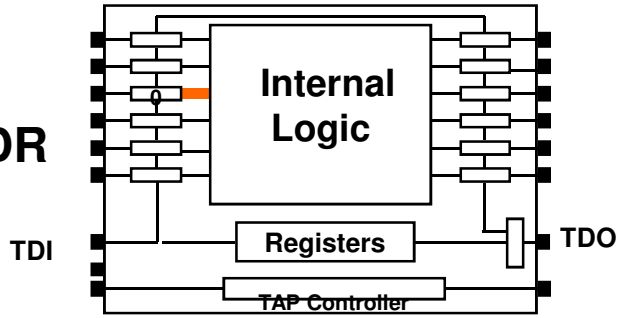

Internal
Logic
TDI
Bypass
Register
(1 bit)
TDO
TAP Controller

INTEST

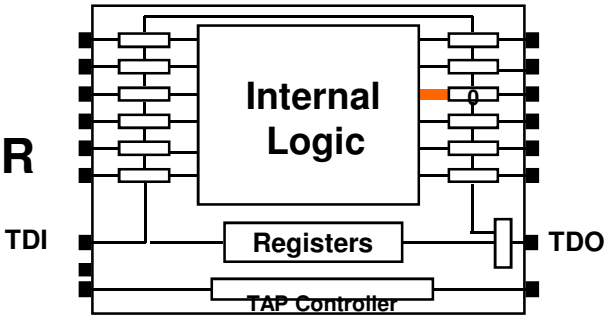
1.Shift-DR



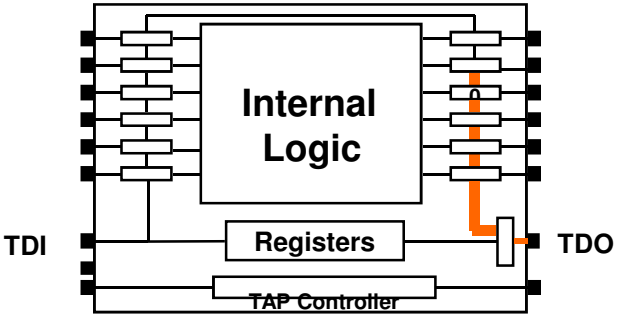
2.Update-DR



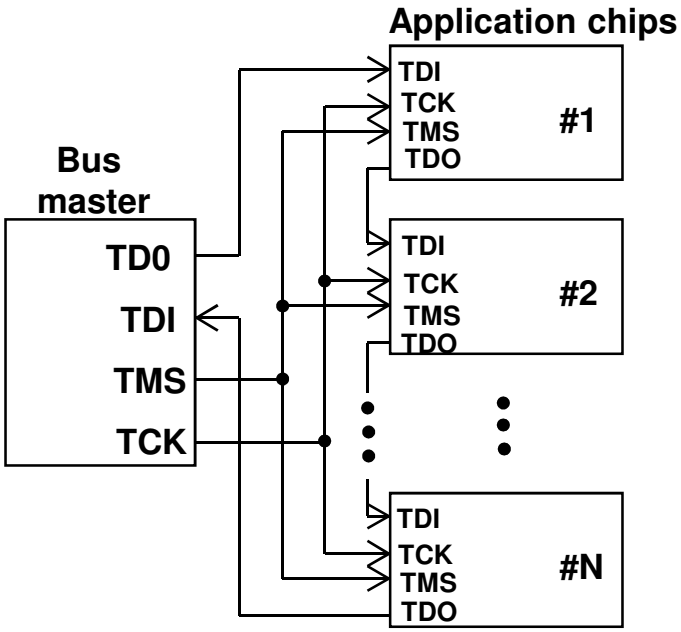
3.Capture-DR



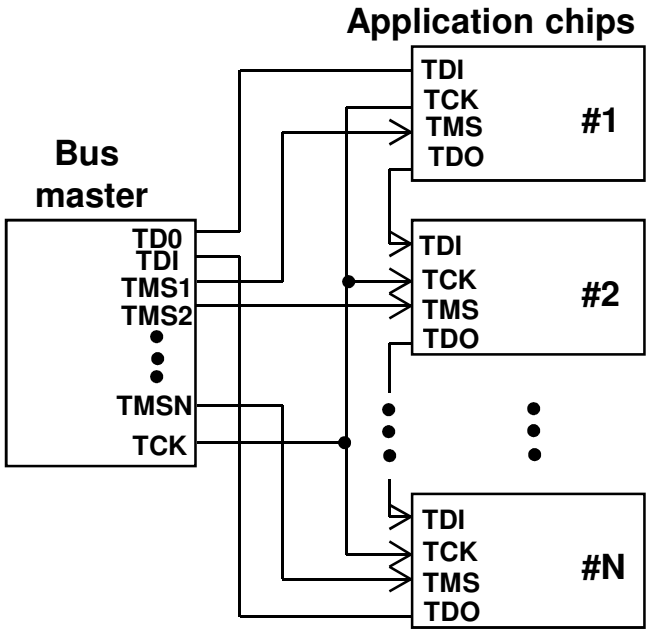
4. Shift-DR



Test Bus Configuration



Ring configuration



Star configuration