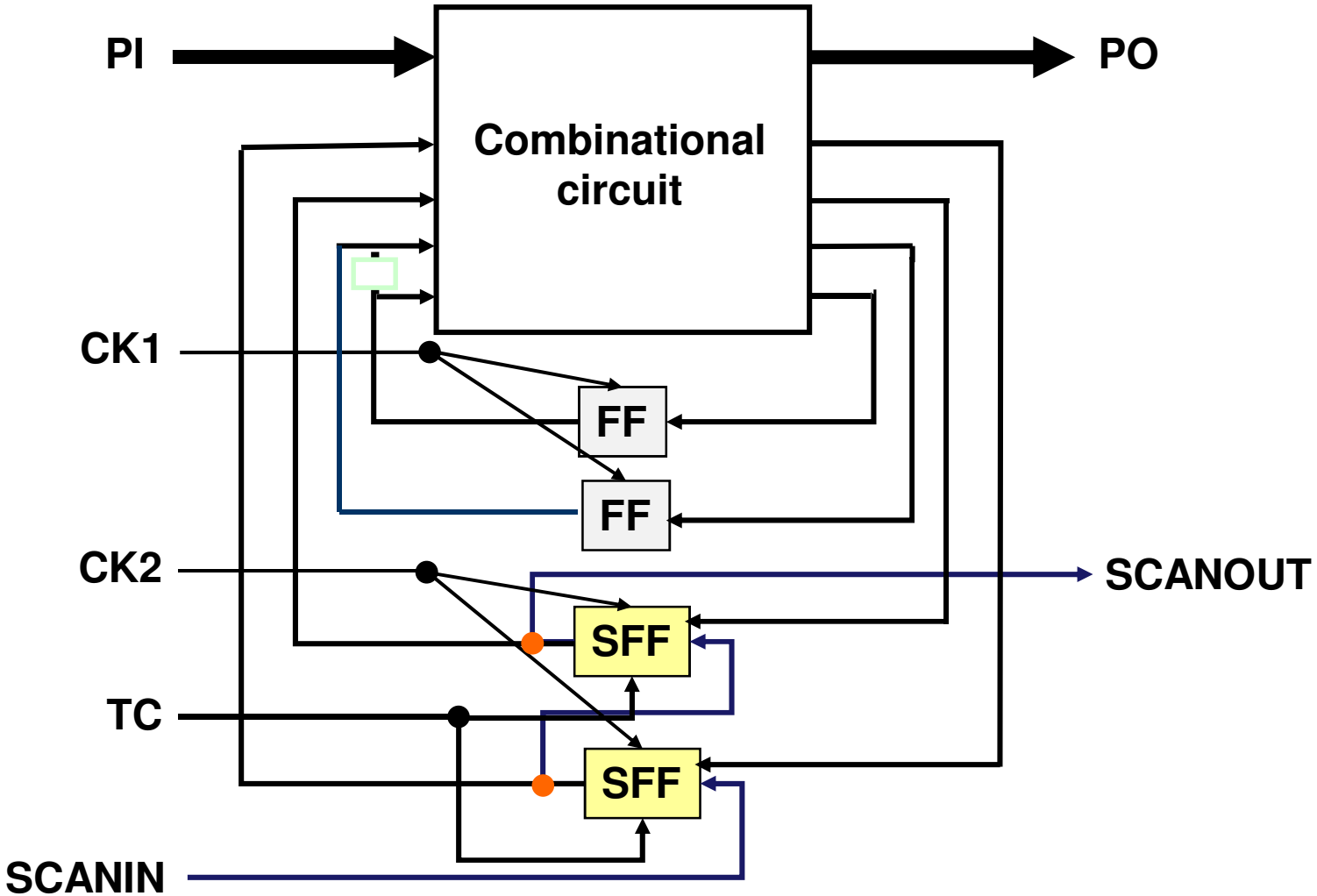
Design for Testability
Part II

Partial-Scan Definition

- A subset of flip-flops is scanned.
- Objectives:
  - Minimize area overhead and scan sequence length, yet achieve required fault coverage.
  - Exclude selected flip-flops from scan:
    - Improve performance
    - Allow limited scan design rule violations
  - Allow automation:
    - In scan flip-flop selection
    - In test generation
  - Shorter scan sequences.

Partial-Scan Architecture



History of Partial-Scan

- Scan flip-flop selection from testability measures, Trischler et al., ITC-80; not too successful.
- Use of combinational ATPG:
  - Agrawal et al., D&T, Apr. 88
    - Functional vectors for initial fault coverage
    - Scan flip-flops selected by ATPG
  - Gupta et al., IEEETC, Apr. 90
    - Balanced structure; may require high scan percentage
- Use of sequential ATPG:
  - Cheng and Agrawal, IEEETC, Apr. 90; Kunzmann and Wunderlich, JETTA, May 90
    - Create cycle-free structure for efficient ATPG

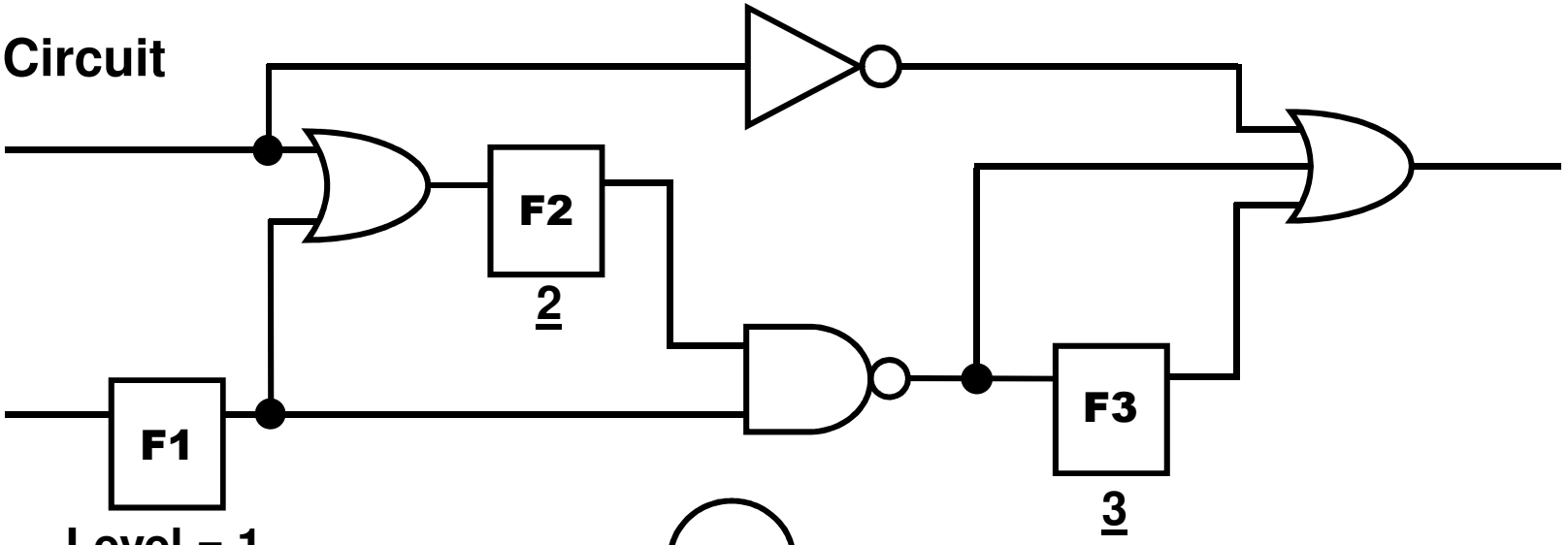
Difficulties in Sequential ATPG

- **Poor initializability.**
- **Poor controllability/observability of state variables.**
- **Gate count, number of flip-flops, and sequential depth do not explain the problem.**
- **Cycles are mainly responsible for complexity.**

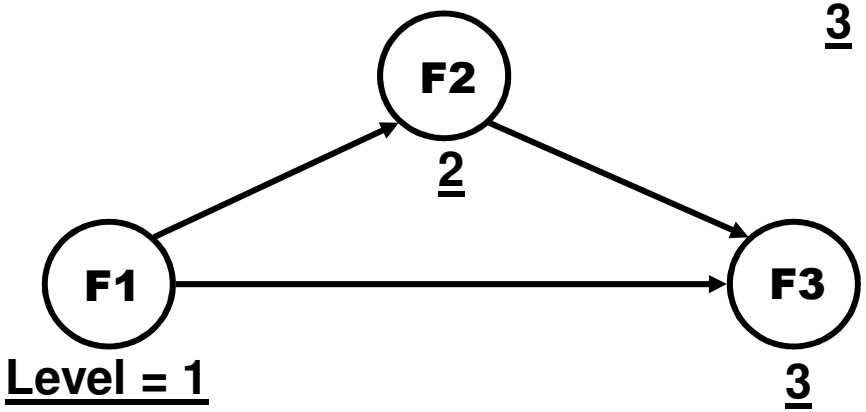
Benchmark Circuits

Circuit	s1196	s1238	s1488	s1494
PI	14	14	8	8
PO	14	14	19	19
FF	18	18	6	6
Gates	529	508	653	647
Structure	Cycle-free	Cycle-free	Cyclic	Cyclic
Sequential depth	4	4	--	--
Total faults	1242	1355	1486	1506
Detected faults	1239	1283	1384	1379
Potentially detected faults	0	0	2	2
Untestable faults	3	72	26	30
Abandoned faults	0	0	76	97
Fault coverage (%)	99.8	94.7	93.1	91.6
Fault efficiency (%)	100.0	100.0	94.8	93.4
Max. sequence length	3	3	24	28
Total test vectors	313	308	525	559
Gentest CPU s (Sparc 2)	10	15	19941	19183

Cycle-Free Example



s - graph



$d_{seq} = 3$

All faults are testable.

Relevant Results

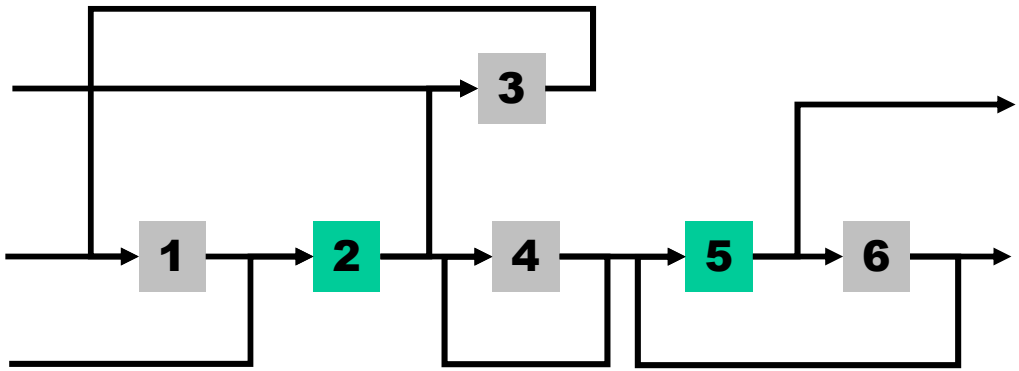
- **Theorem 1:**
  - **A cycle-free circuit is always initializable. It is also initializable in the presence of any non-flip-flop fault.**
- **Theorem 2:**
  - **Any non-flip-flop fault in a cycle-free circuit can be detected by at most d_{seq} + 1 vectors.**
- **ATPG complexity:**
  - **To determine that a fault is untestable in a cyclic circuit, an ATPG program using 9-valued logic may have to analyze 9^{Nff} time-frames, where Nff is the number of flip-flops in the circuit.**

A Partial-Scan Method

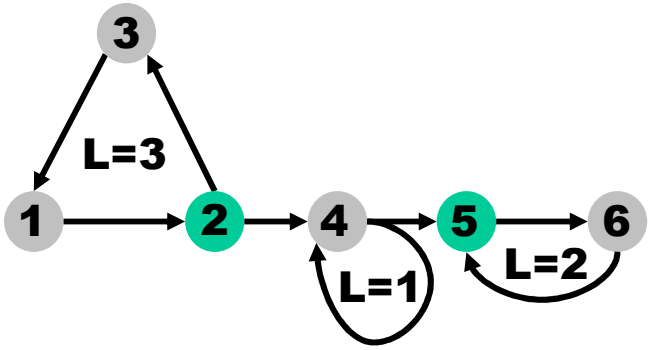
- Select a minimal set of flip-flops for scan to eliminate all cycles.
- Alternatively, to keep the overhead low only long cycles may be eliminated.
- In some circuits with a large number of self-loops, all cycles other than self-loops may be eliminated.

The MFVS Problem

- **For a directed graph find a set of vertices with smallest cardinality such that the deletion of this vertex-set makes the graph acyclic.**
- **The *minimum feedback vertex set (MFVS)* problem is NP-complete; practical solutions use heuristics.**
- **A secondary objective of minimizing the depth of acyclic graph is useful.**



A 6-flip-flop circuit



s-graph

Test Generation

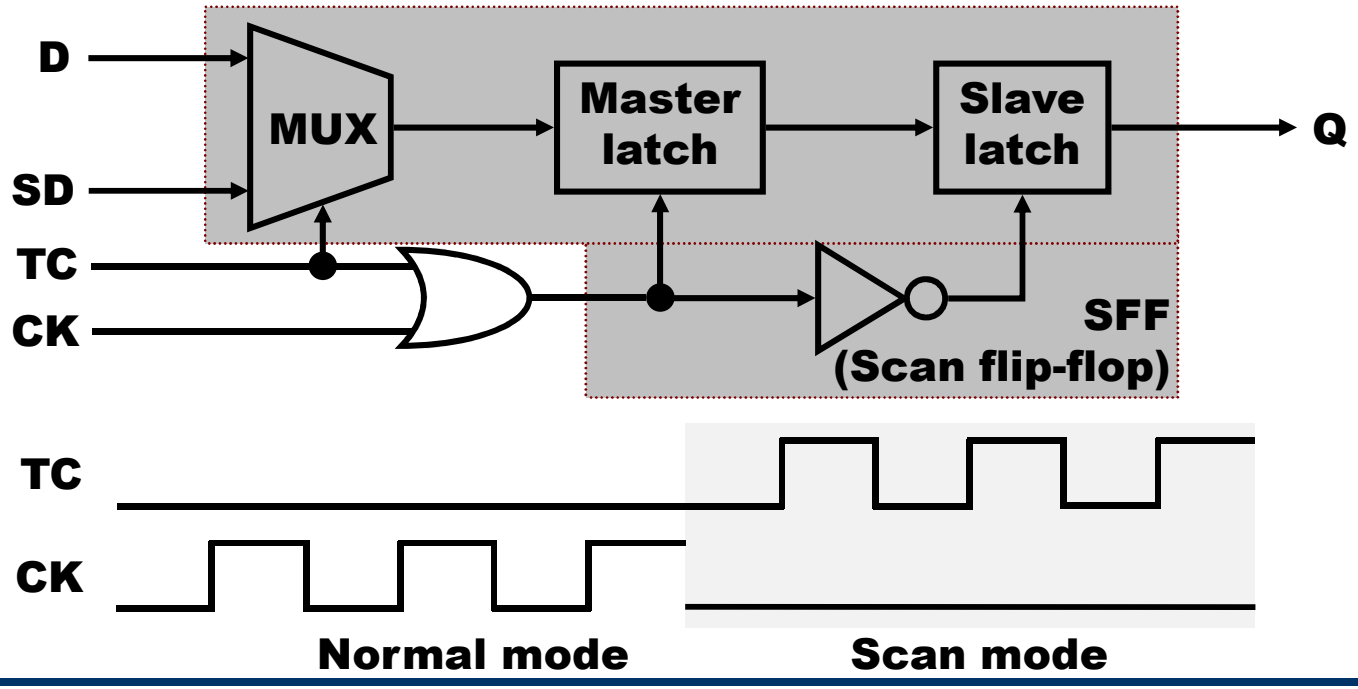
- Scan and non-scan flip-flops are controlled from separate clock PIs:
  - Normal mode – Both clocks active
  - Scan mode – Only scan clock active
- Sequential ATPG model:
  - Scan flip-flops replaced by PI and PO
  - Sequential ATPG program used for test generation
  - Scan register test sequence, 001100…, of length $n_{sff} + 4$ applied in the scan mode
  - Each ATPG vector is preceded by a scan-in sequence to set scan flip-flop states
  - A scan-out sequence is added at the end of each vector sequence
- Test length = $(n_{ATPG} + 2)\, n_{sff} + n_{ATPG} + 4$ clocks

Partial vs. Full Scan: S5378

	Original	Partial-scan	Full-scan
Number of combinational gates	2,781	2,781	2,781
Number of non-scan flip-flops (10 gates each)	179	149	0
Number of scan flip-flops (14 gates each)	0	30	179
Gate overhead	0.0%	2.63%	15.66%
Number of faults	4,603	4,603	4,603
PI/PO for ATPG	35/49	65/79	214/228
Fault coverage	70.0%	93.7%	99.1%
Fault efficiency	70.9%	99.5%	100.0%
CPU time on SUN Ultra II 200MHz processor	5,533 s	727 s	5 s
Number of ATPG vectors	414	1,117	585
Scan sequence length	414	34,691	105,662

Flip-flop for Partial Scan

- Normal scan flip-flop (SFF) with multiplexer of the LSSD flip-flop is used.
- Scan flip-flops require a separate clock control:
  - Either use a separate clock pin
  - Or use an alternative design for a single clock pin

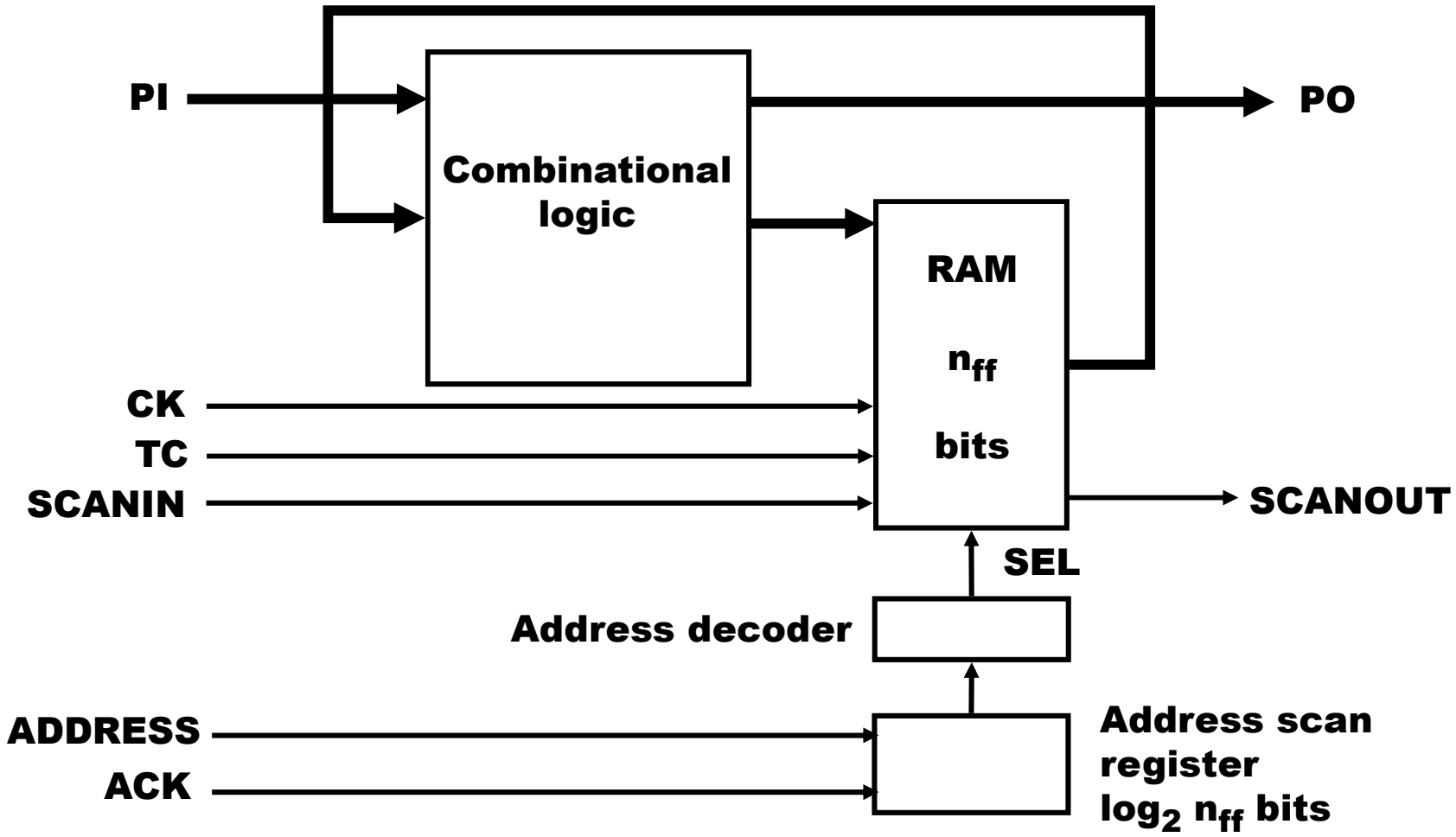


Summary: Partial Scan

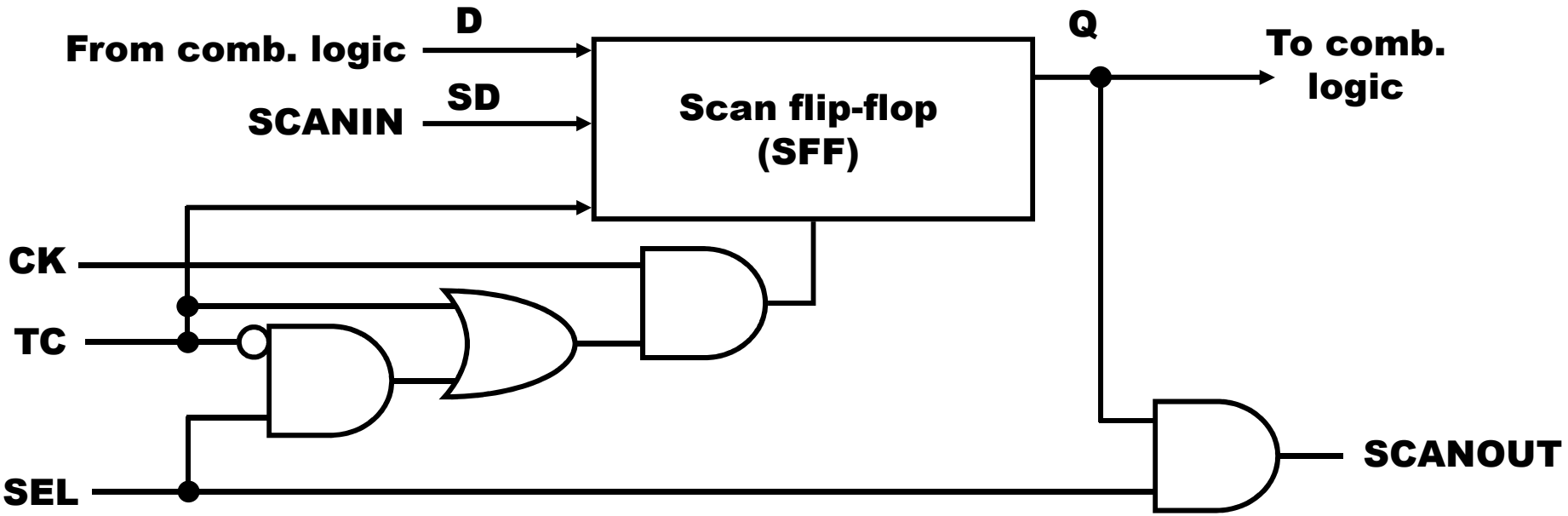
- Partial-scan is a generalized scan method; scan can vary from 0 to 100%.
- Elimination of long cycles can improve testability via sequential ATPG.
- Elimination of all cycles and self-loops allows combinational ATPG.
- Partial-scan has lower overheads (area and delay) and reduced test length.
- Partial-scan allows limited violations of scan design rules, e.g., a flip-flop on a critical path may not be scanned.

Random Access Scan

Random-Access Scan (RAS)



RAS Flip-Flop (RAM Cell)

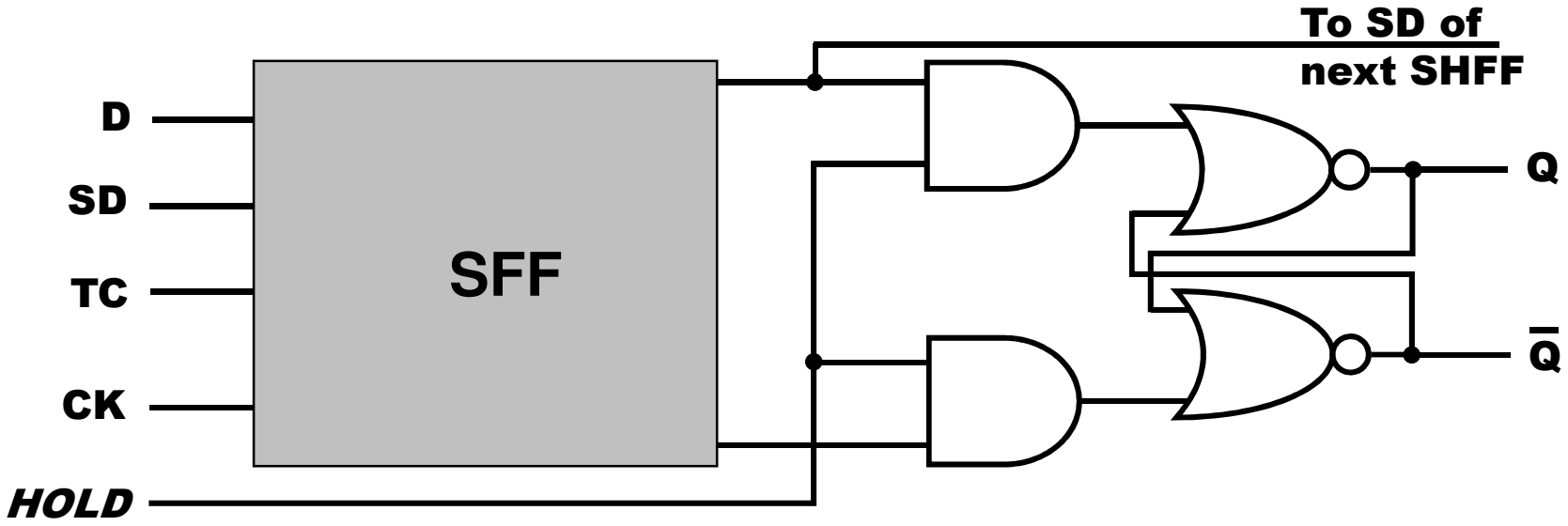


RAS Applications

- **Logic test: reduced test length.**
- **Delay test: Easy to generate *single-input-change* (SIC) delay tests.**
- **Advantage: RAS may be suitable for certain architecture, e.g., where memory is implemented as a RAM block.**
- **Disadvantages:**
  - **Not suitable for random logic architecture**
  - **High overhead – gates added to SFF, address decoder, address register, extra pins and routing**

Scan-Hold Flip-Flop

Scan-Hold Flip-Flop (SHFF)



- The control input *HOLD* keeps the output steady at previous state of flip-flop.

- **Applications:**
  - **Reduce power dissipation during scan**
  - **Isolate asynchronous parts during scan test**
  - **Delay testing**