Design for Testability

Basic Concept

- **Design for testability (DFT)**
  - **Design techniques that make test generation and test application cost-effective.**
- **DFT methods for digital circuits:**
  - **Ad-hoc methods**
  - **Structured methods**
    - **Scan path**
    - **Level sensitive scan design**
    - **Random access scan**
    - **……**

Ad-Hoc DFT Methods

- Good design practices learned through experience are used as guidelines:
  - Don't-s and Do-s
    - Avoid asynchronous (unclocked) feedback.
    - Avoid delay dependant logic.
    - Avoid parallel drivers.
    - Avoid monostables and self-resetting logic.
    - Avoid gated clocks.
    - Avoid redundant gates.

- **Avoid high fanin fanout combinations.**
- **Make flip-flops initializable.**
- **Separate digital and analog circuits.**
- **Provide test control for difficult-to-control signals.**

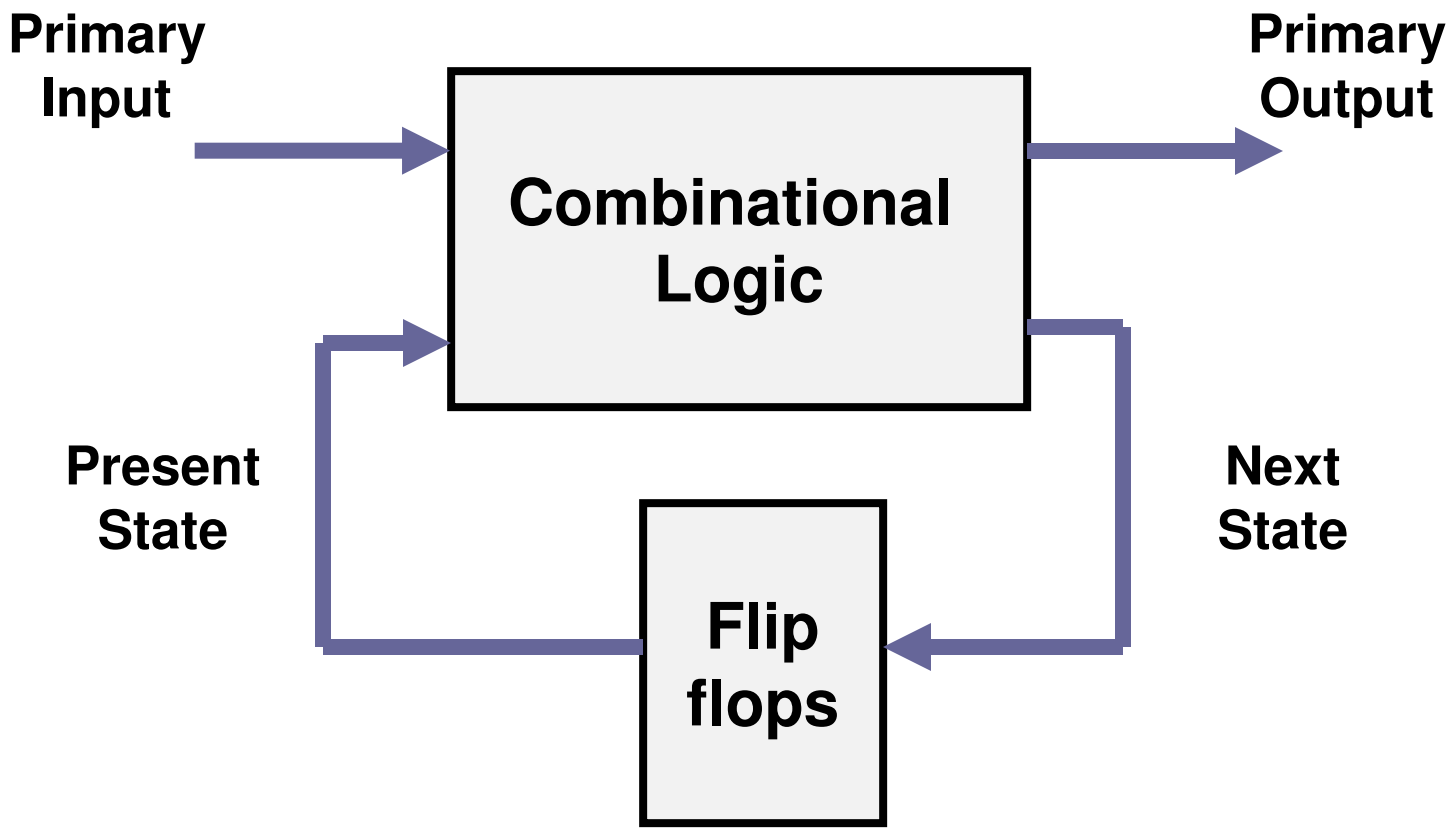
Ad-hoc Methods :: Drawbacks

- Experts and tools are not always available.
- Test generation is often manual, and so high fault coverage is not guaranteed.
- Design iterations may be required.
- Difficult to automate.

Structured Methods

- **Helps to provide good controllability and observability of internal state variables for testing.**
  - **Converts the sequential test generation problem into a combinational one.**
- **Major approaches:**
  - **Scan path**
  - **LSSD**
  - **Random access scan**
  - **Variations to above …….**

A Sequential Circuit



Scan Path Design

- **Basic Problem**
  - **Test generation for sequential circuits is difficult.**
- **Objective**
  - **Make all the flip-flops directly controllable and observable.**
- **What do we gain?**
  - **Combinational circuit test generation can be used.**
  - **A few additional tests to test the flip-flops (shift register).**

Scan Design (contd.)

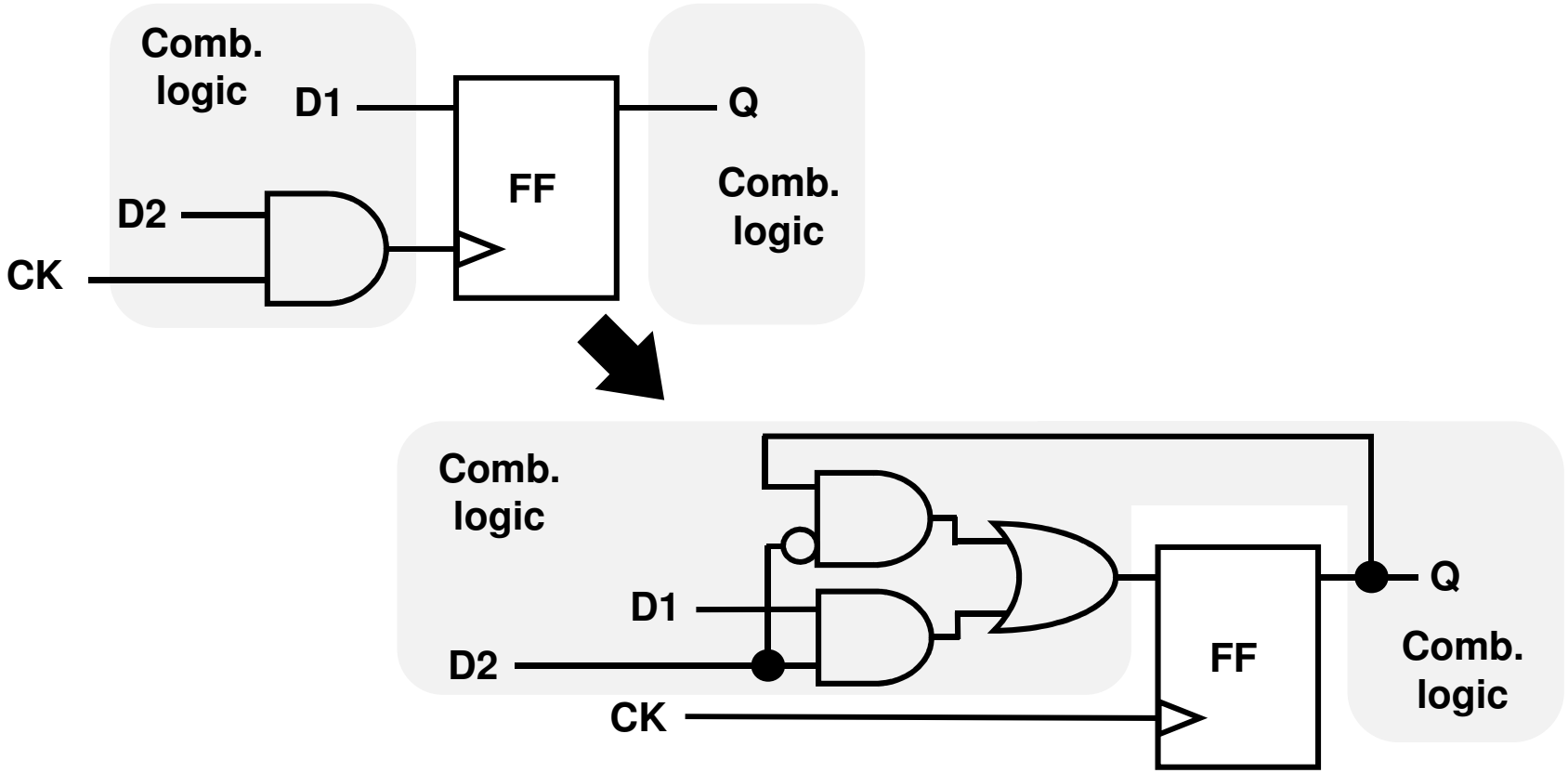
- **Pre-specified design rules.**
- **Test structure added to the verified design.**
  - **Add one (or more) *test control* (TC) primary input.**
  - **Replace flip-flops by *scan flip-flops*.**
  - **Connect scan flip-flops to form one or more *shift registers* in test mode.**
  - **Add SCANIN and SCANOUT pins to shift register.**
- **Add *shift register test* and convert ATPG tests into *scan sequences* for use in manufacturing test.**

Scan Design Rules

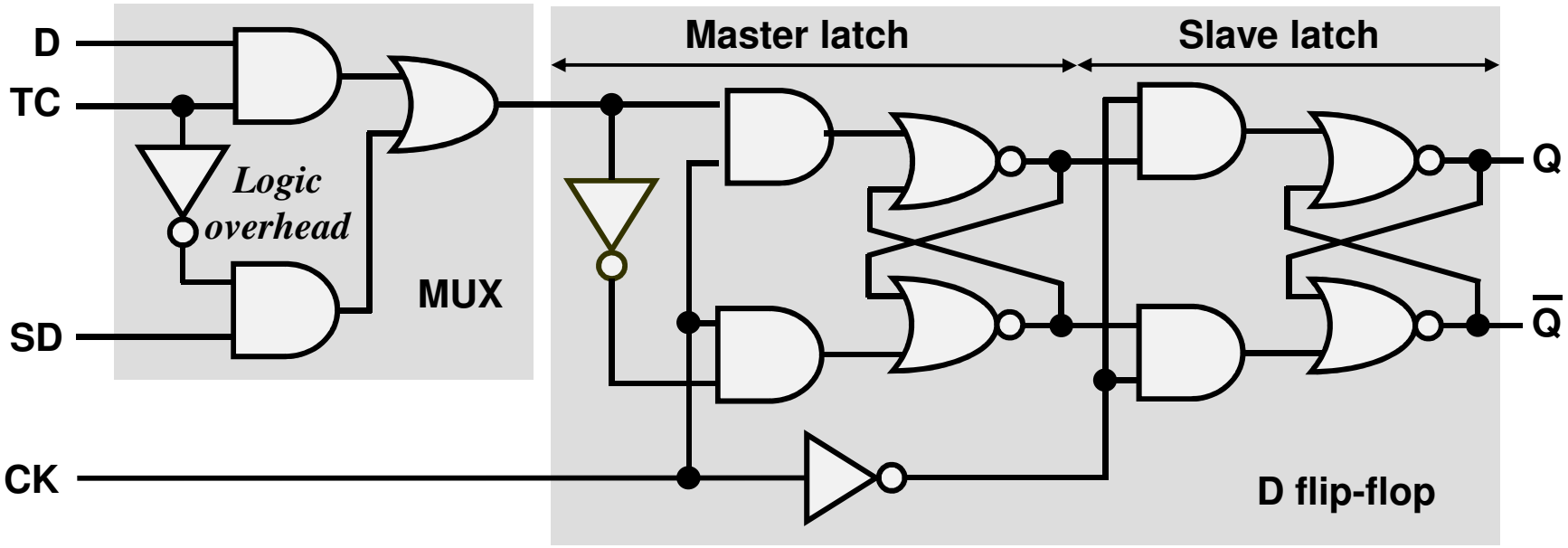
- Use only clocked D-type master-slave flip-flops for all state variables.
- At least one PI pin must be available for test; more pins, if available, can be used.
- All clocks must be controlled from PIs.
  - Necessary for flip-flops to work in scan registers.
- Clocks must not feed data inputs of flip-flops.
  - May lead to race condition.

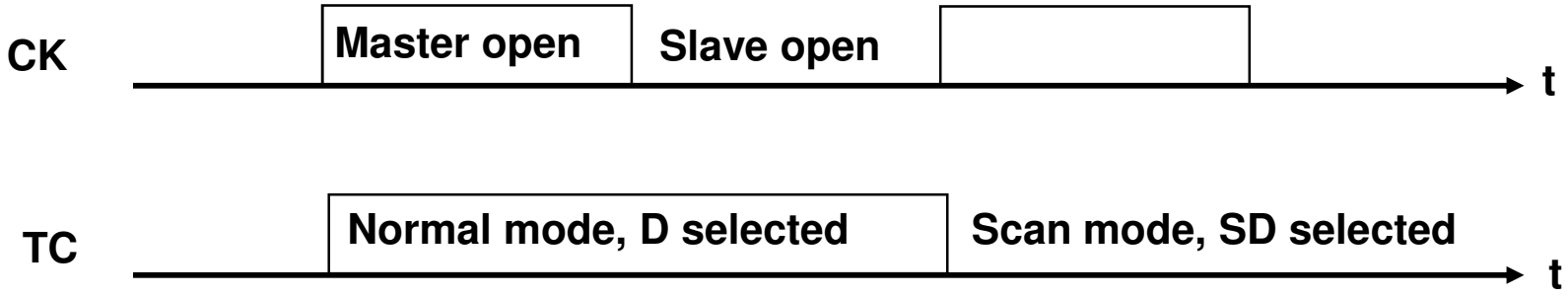
Correcting a Rule Violation

- **All clocks must be controlled from PIs.**

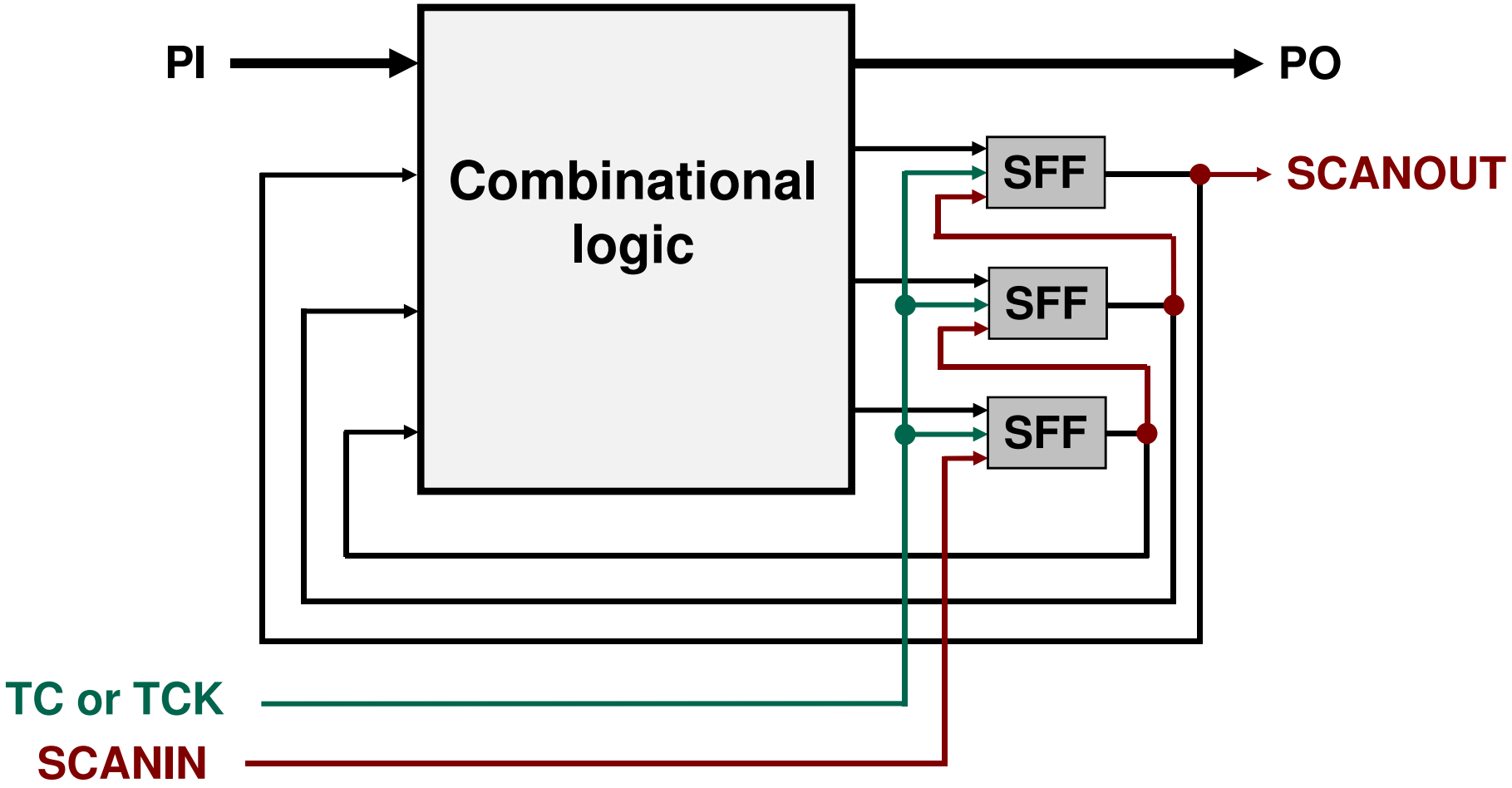


Scan Flip-Flop (master-slave)





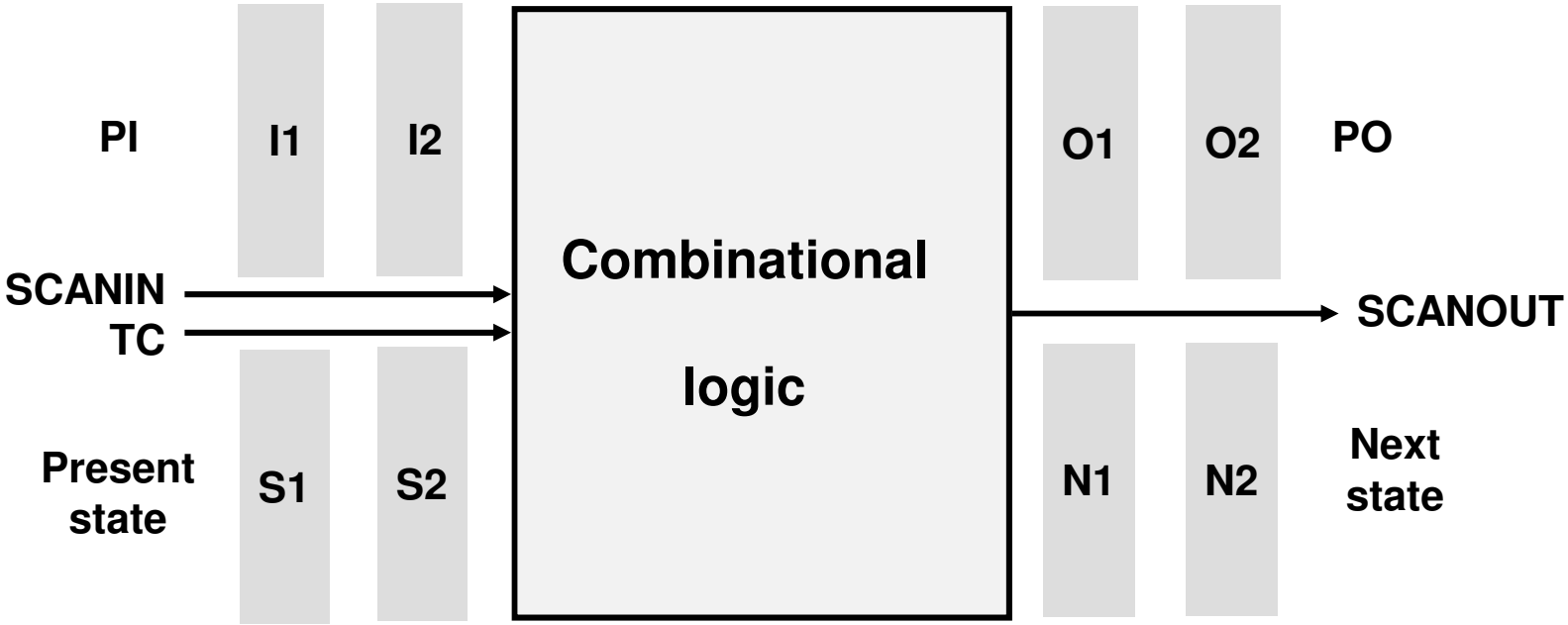
Adding Scan Structure



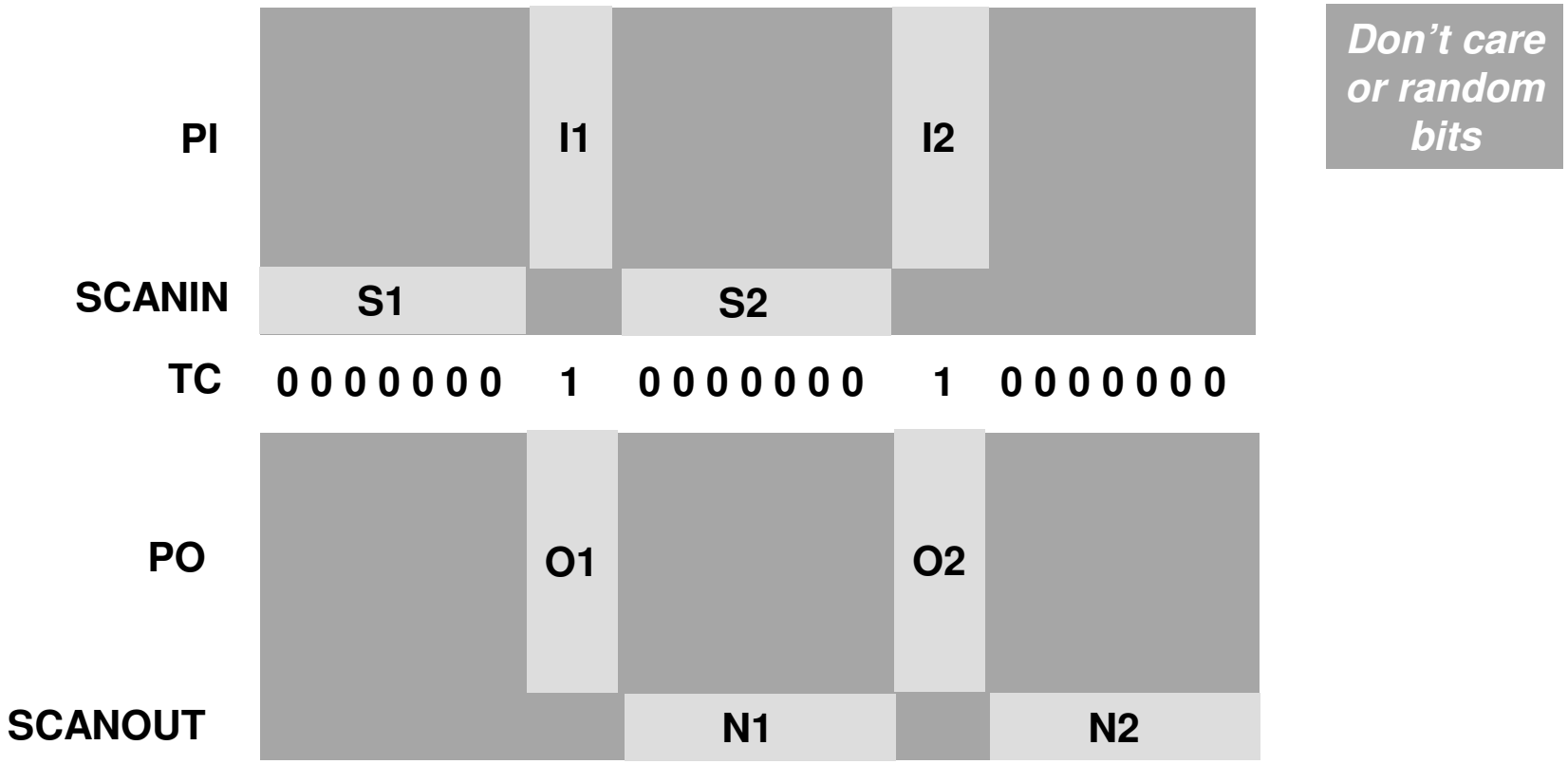
- **Application of the test vectors:**

PI	Present State	PO	Next State
I1	S1	O1	N1
I2	S2	O2	N2
I3	S3	O3	N3
…	…	…	…

Combinational Test Vectors



Combinational Test Vectors



- **Scan sequence length:**

$$(n_s + 1)\, n_c + n_s \quad \textit{clock periods}$$

where n_c *: number of combinational test vectors*

n_s *: number of scan flip-flops*

An example: the I/O specifications

3 inputs, 2 outputs, and 3 state variables

PI	Present State	PO	Next State
0 1 0	1 0 0	0 1	1 0 1
0 1 1	0 1 0	1 1	0 0 1
1 0 1	1 0 0	1 0	1 1 1
0 0 1	1 0 1	0 1	0 1 0

contd. : corresponding scan sequence

Clock	PI	SCANIN	TC	PO	SCANOUT
1	xxx	1	0	xx	x
2	xxx	0	0	xx	x
3	xxx	0	0	xx	x
4	010	x	1	01	x
5	xxx	0	0	xx	1
6	xxx	1	0	xx	0
7	xxx	0	0	xx	1
8	011	x	1	11	x

Scan Testing Time

- **Scan register has to be tested prior to the application of scan test sequences.**
  - **A shift sequence 00110011… of length n_s+4.**
  - **Produces all possible transitions in all flip-flops.**
- **Total scan test length:**

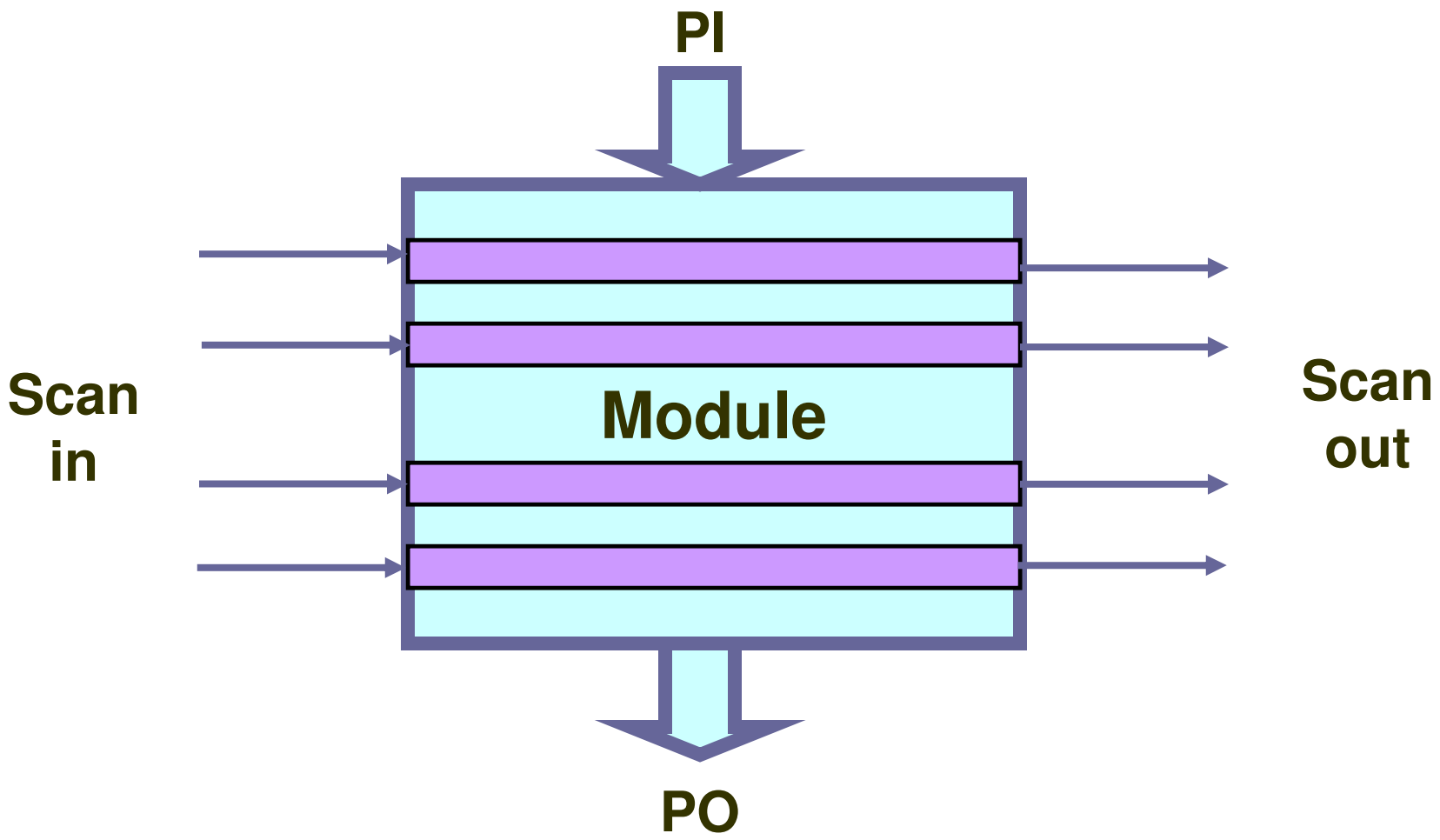
  $(n_s + 1)\, n_c + n_s + (n_s + 4)$

  n_s : number of scan flip-flops

  n_c : number of combinational test vectors

  n_s=2000, n_c=500 ➔ Test length = 10^6

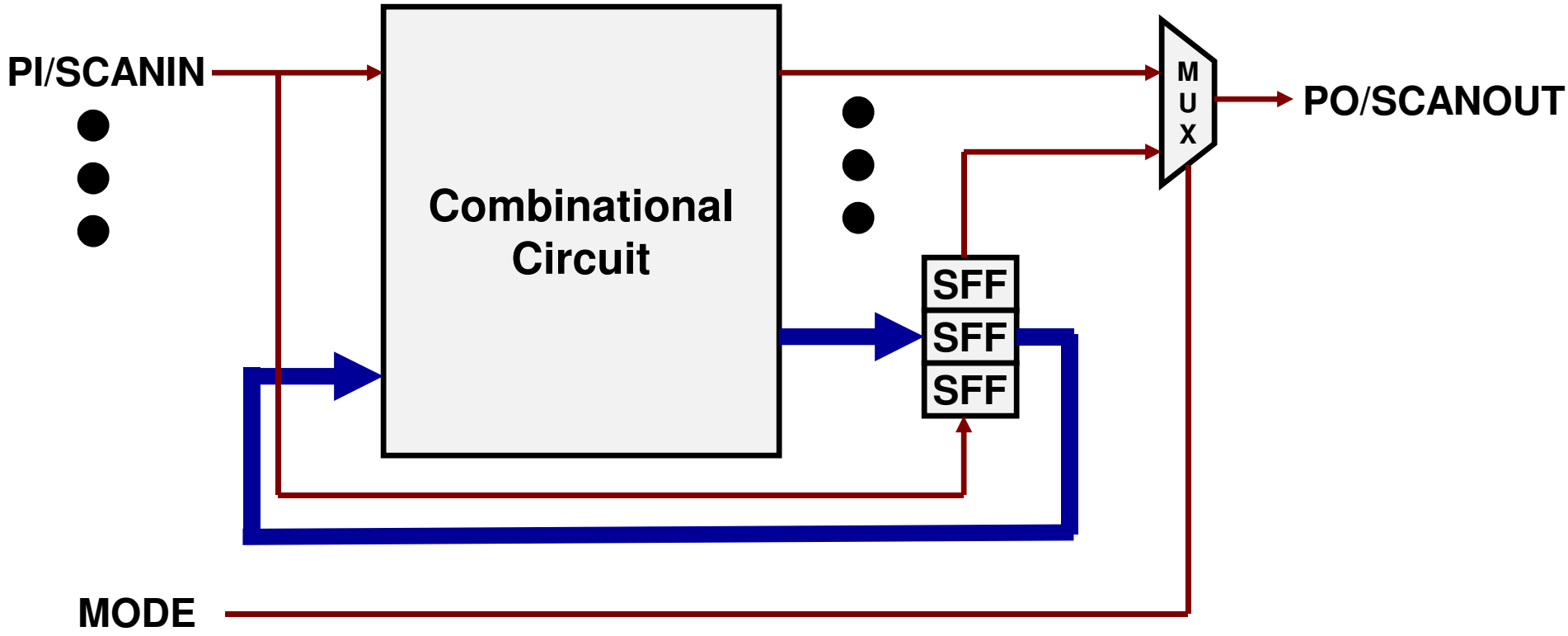
A Typical Module With Scan Chains



Multiple Scan Paths

- **Scan flip-flops can be distributed among any number of shift registers, each having a separate *SCANIN* and *SCANOUT* pin.**
  - **PI and PO pins can be shared with SCANIN and SCANOUT pins respectively.**
- **Test sequence length is determined by the longest scan shift register.**
- **Just one test control (TC) pin is essential.**

Multiple Scan Path Example



Only one scan path is shown; others can be added similarly

Other Issues

- Multiple scan paths can reduce test application time.
- Scan overhead:
  - One additional pin (TC)
    - Other pins can be multiplexed with functional input and output pins.
  - Area overhead
    - Replacing flip-flops by scan flip-flops.
  - Performance overhead
    - Additional MUX-es in critical path.
    - Increase in fanout for the flip-flops.

Scan Overheads

- **IO pins:**
  - **One pin necessary.**
- **Area overhead:**

  $$\textit{Gate overhead} = [4\, n_s / (n_g + 10 n_s)] \times 100\%$$

  where n_g = number of *gates in combinational logic*

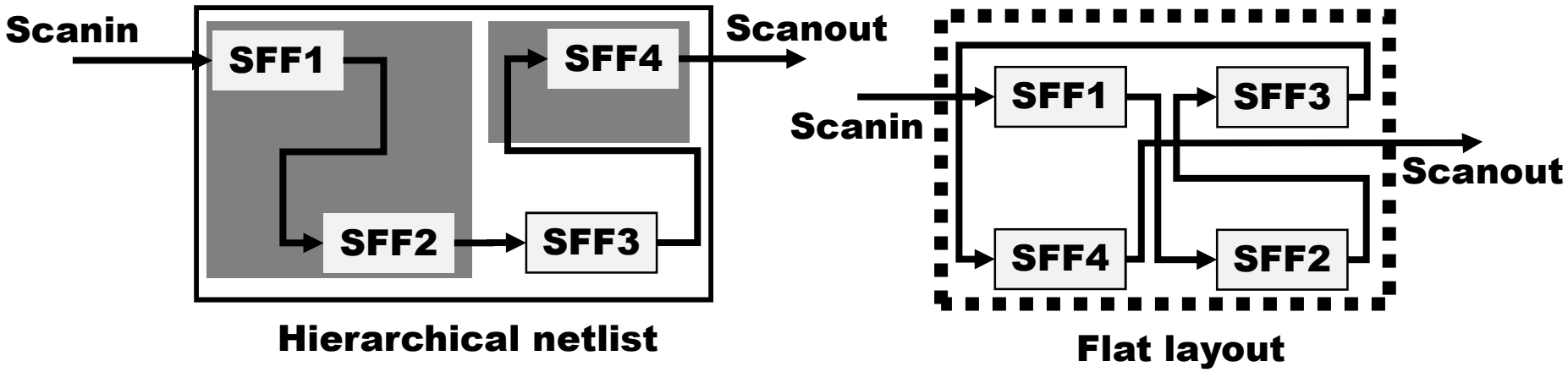
  n_s = number of *flip-flops*

  - **Example:**
    - **n_g = 100k gates, n_s = 2k *flip-flops*, overhead = 6.7%.**
  - **More accurate estimate must consider scan wiring and layout area.**

- **Performance overhead:**
  - **Multiplexer delay added in combinational path; approx. two gate-delays.**
  - **Flip-flop output loading due to one additional fanout; approx. 5-6%.**

Hierarchical Scan

- Scan flip-flops are chained within subnetworks before chaining subnetworks.
- Advantages:
  - Automatic scan insertion in netlist
  - Circuit hierarchy preserved – helps in debugging and design changes
- Disadvantage: Non-optimum chip layout.



ATPG Example: S5378

	Original	Full-scan
Number of combinational gates	2,781	2,781
Number of non-scan flip-flops (10 gates each)	179	0
Number of scan flip-flops (14 gates each)	0	179
Gate overhead	0.0%	15.66%
Number of faults	4,603	4,603
PI/PO for ATPG	35/49	214/228
Fault coverage	70.0%	99.1%
Fault efficiency	70.9%	100.0%
CPU time on SUN Ultra II, 200MHz processor	5,533 s	5 s
Number of ATPG vectors	414	585
Scan sequence length	414	105,662

Summary

- Scan is the most popular DFT technique:
  - Rule-based design
  - Automated DFT hardware insertion
  - Combinational ATPG
- Advantages:
  - Design automation
  - High fault coverage; helpful in diagnosis
  - Hierarchical – scan-testable modules are easily combined into large scan-testable systems
  - Moderate area (~10%) and speed (~5%) overheads

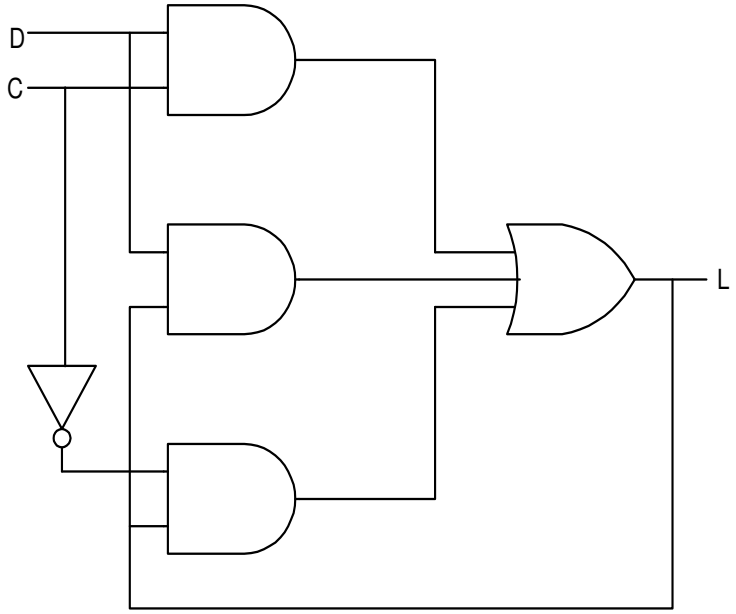
- **Disadvantages:**
  - **Large test data volume and long test time**
  - **Basically a slow speed (DC) test**

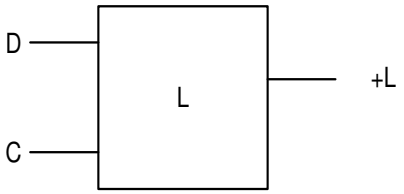
Level Sensitive Scan Design

- Similar to scan path in concept; uses level sensitive latches.
- Main issues:
  - Absence of races and hazards.
  - Insensitive to rise time, fall time, delay, etc.
  - Lower hardware complexity as compared to scan path design.
  - More complex design rules.

LSSD

Polarity-Hold Latch:



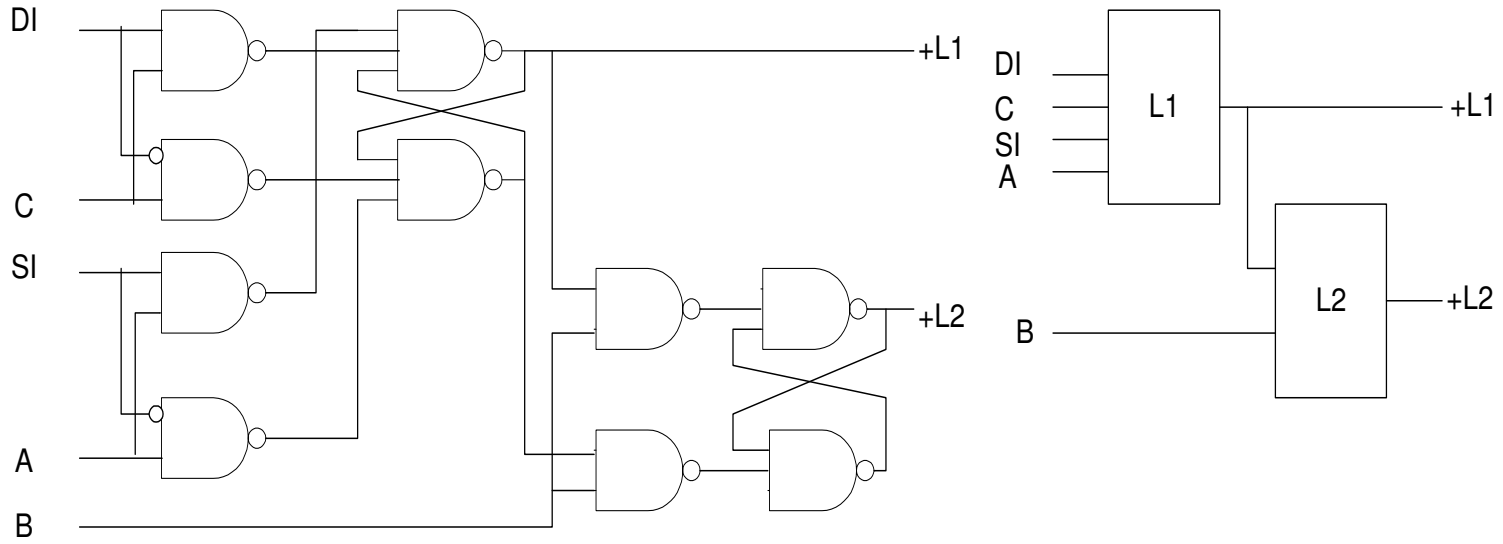


C	D	+L
0	0	L
0	1	L
1	0	0
1	1	1

- **The correct change of the latch output (L) is not dependent on the rise/fall time of C, but only on C being '1' for a period of time ≥ data propagation and stabilization time.**

LSSD

Polarity-Hold Shift-Register Latch (SRL):

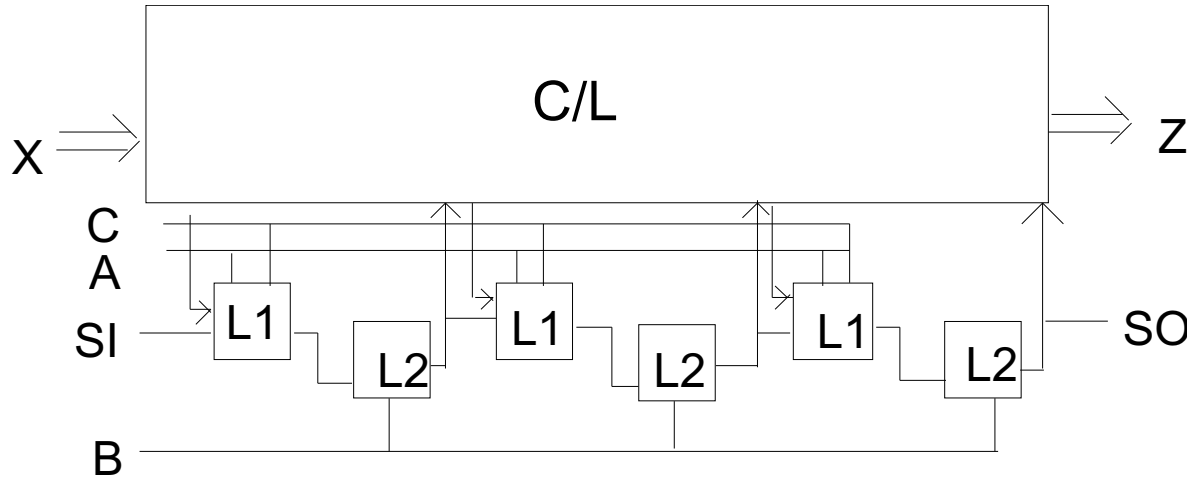


- **Normal mode: A = B =0, C =0 → 1.**
- **SR (test) mode: C =0, AB = 10 → 01 to shift SI through L_1 and L_2.**

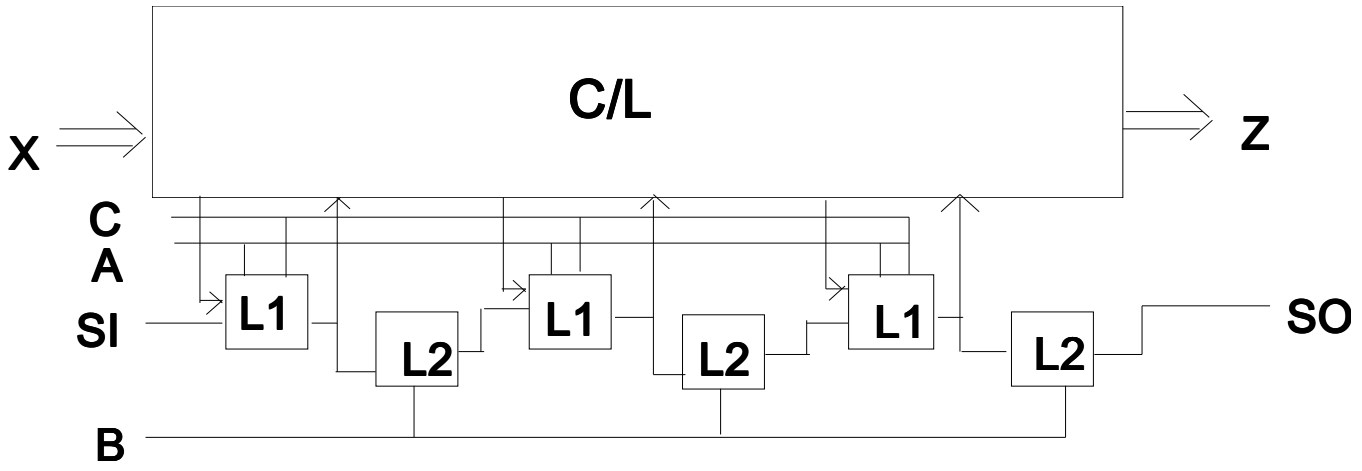
LSSD

- **Polarity-Hold, hazard-free, and level-sensitive.**
- **To be race-free, clocks C & B as well as A & B must be non-overlapping.**
- **Avoids performance degradation introduced by the MUX in shift-register modification.**

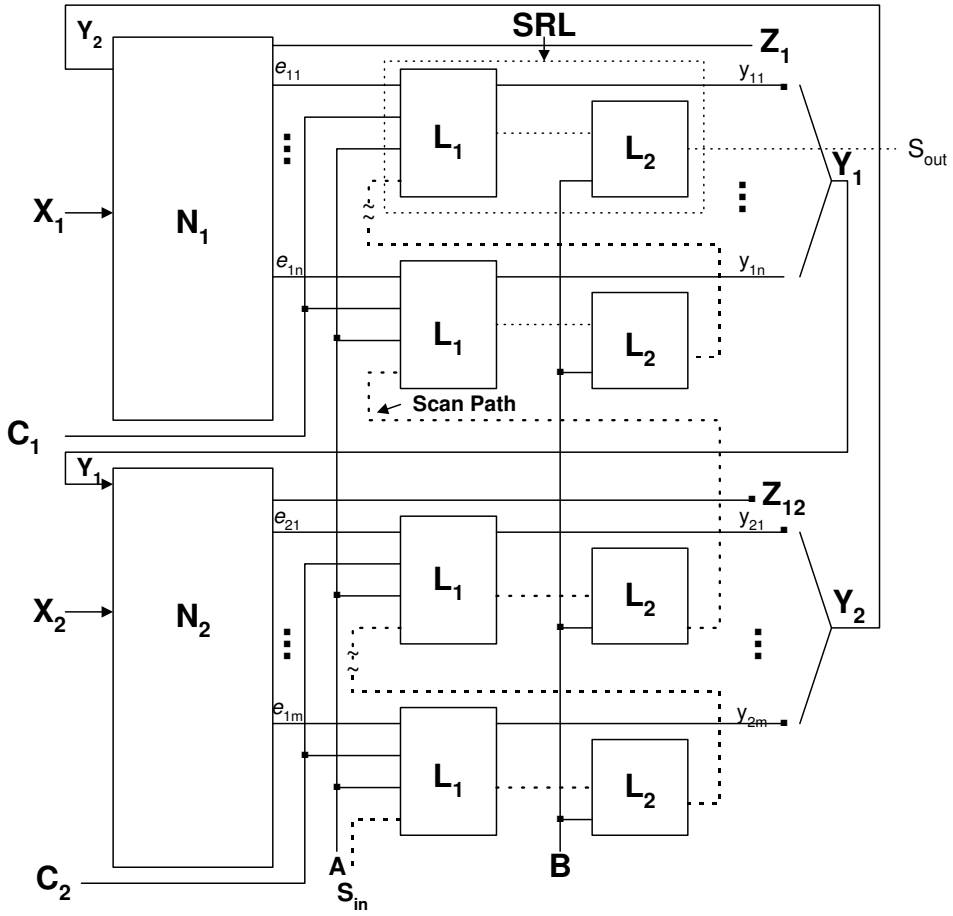
Double-Latch LSSD



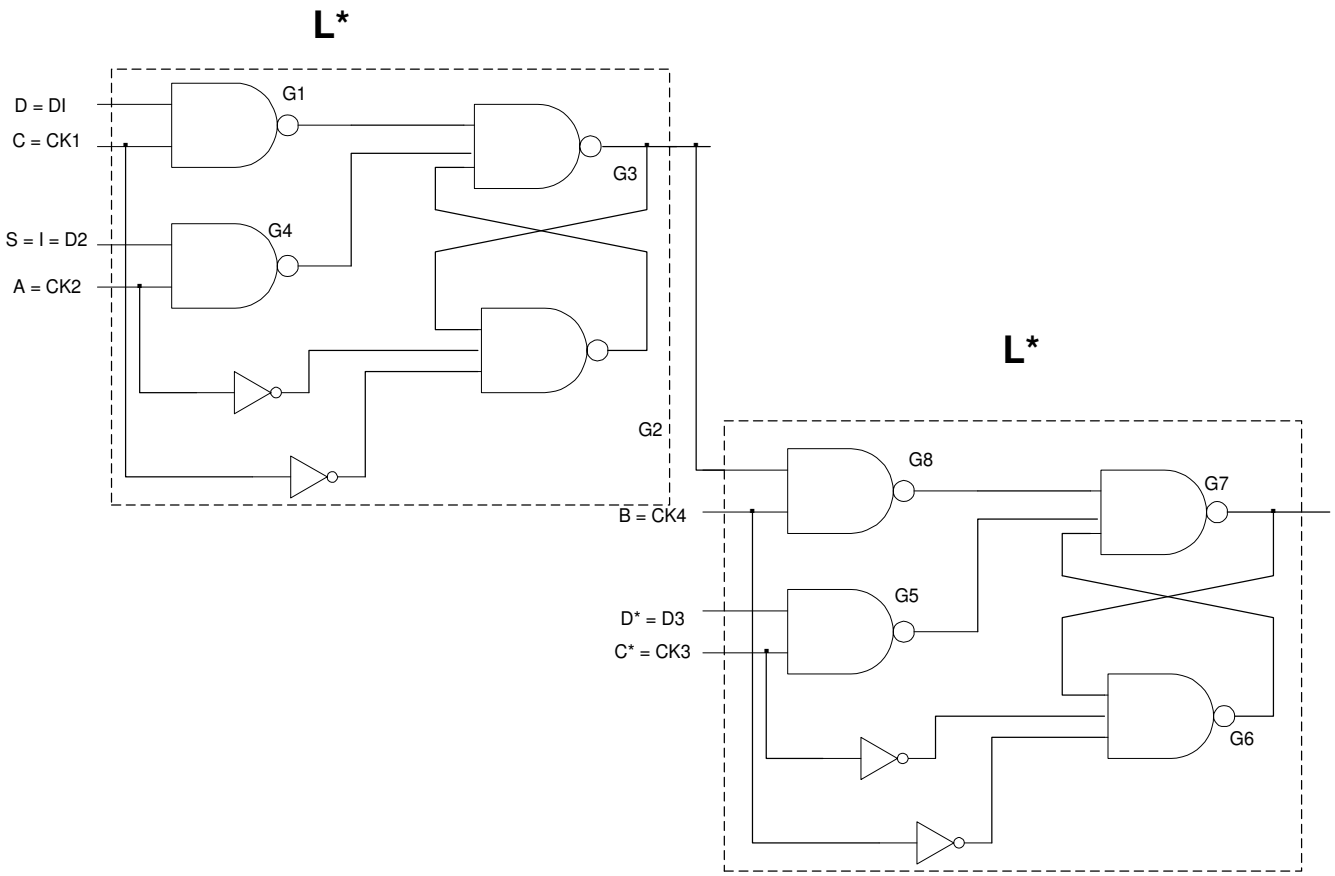
Single-Latch LSSD



Single-Latch LSSD With Conventional SRLs

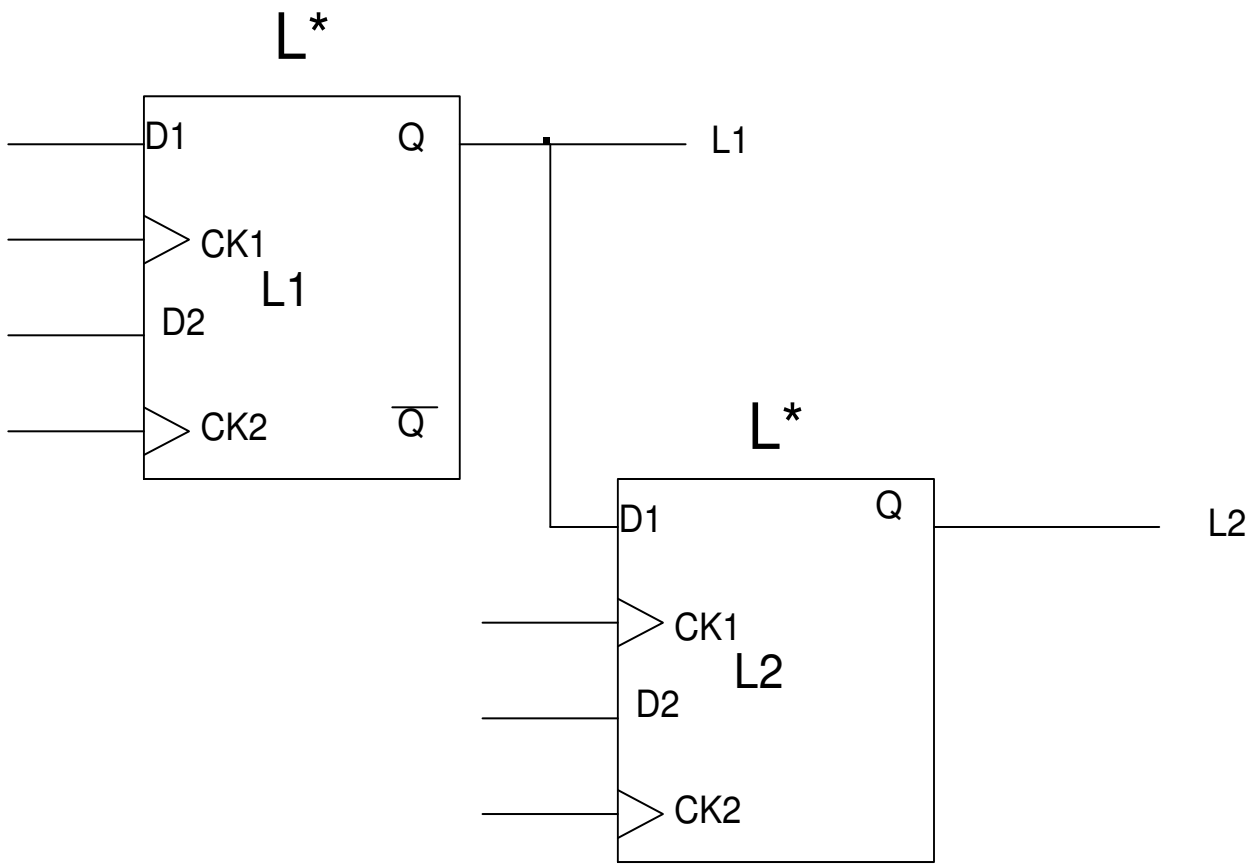


SRL Using Two-Port L_2^*



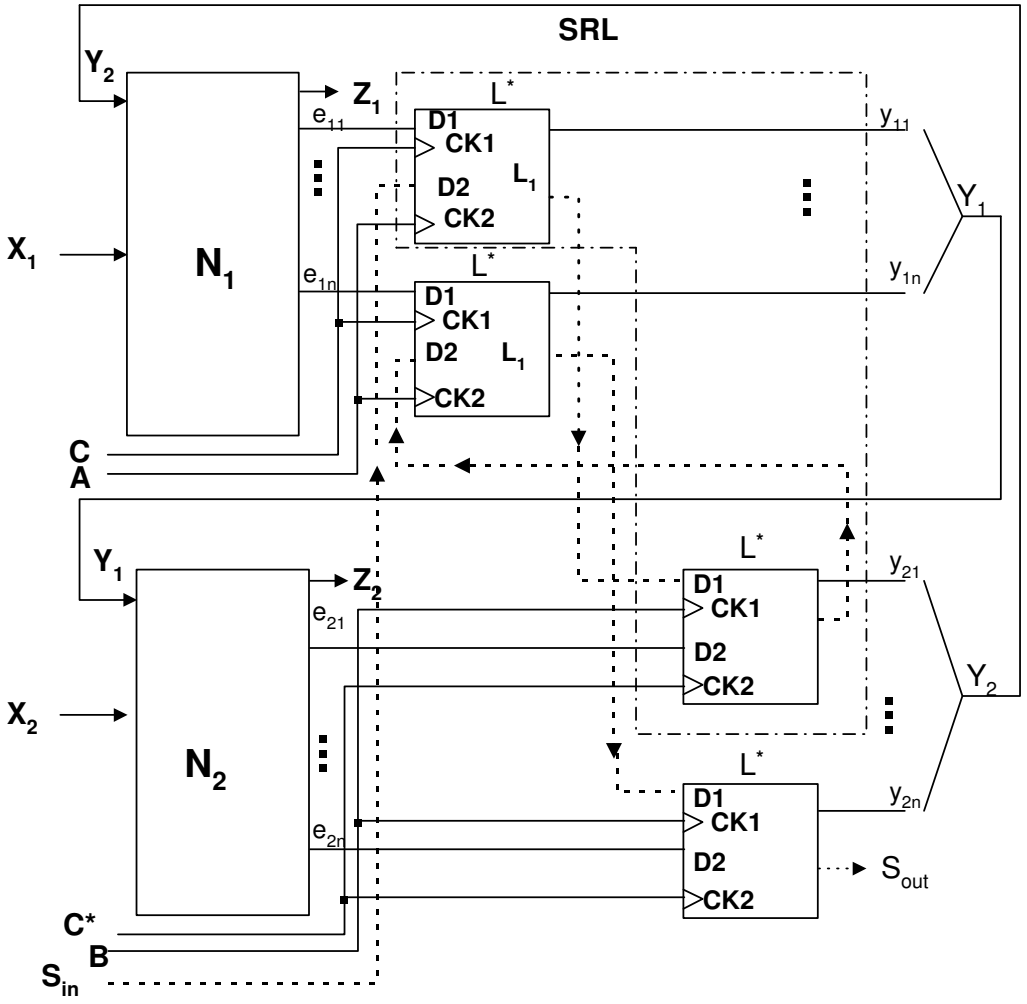
(a) Gate model

SRL Using Two-Port L_2^*



(b) Symbol

Single-Latch LSSD With L_2* Latches



LSSD Design Rules

1. Internal storage elements must be polarity-hold latches.
2. Latches can be controlled by 2 or more non-overlapping clocks that satisfy:
   - A latch X may feed the data port of another latch Y iff the clock that sets the data into Y does not clock X.
   - A latch X may gate a clock C to produce a gated clock C_g , which drives another latch Y iff C_g , or any other clock C_{1g} , produced from C_g , does not clock X.

LSSD Design Rules (contd.)

3. There must exist a set of clock primary inputs from which the clock inputs to all SRLs are controlled either through (1) single-clock distribution tree, or (2) logic that is gated by SRLs and/or non-clock primary inputs. In addition, the following conditions must hold:
   - All clock inputs to SRLs must be OFF when clock PIs are OFF.
   - Any SRL clock input must be controlled from one or more clock PIs.
   - No clock can be ANDed with either the true or the complement of another clock.

LSSD Design Rules (contd.)

4. Clock PIs cannot feed the data inputs to latches, either directly or through combinational logic.
5. Every system latch must be part of an SRL; each SRL must be part of some scan chain.
6. A scan state exists under the following conditions:
   - Each SRL or scan-out PO is a function of only the preceding SRL or scan-in PI in its scan chain during the scan operation.
   - All clocks except the shift clocks are disabled at the SRL inputs.

LSSD Design Rules (contd.)

7. Any shift clock to an SRL can be turned ON or OFF by changing the corresponding clock PI.
   - A network that satisfies rules 1-4 is level-sensitive.
   - Race-free operation is guaranteed by rules 2(1) & 4.
   - Rule 3 allows a tester to turn off system clocks and use the shift clocks to force data into and out of the scan chain.
   - Rules 5 & 6 are used to support scan.

Advantages With LSSD

- Correct operation independent of AC characteristics.
- Reducing FSM to C/L as far as testing is concerned.
- Eliminating hazards & races; simplifying test generation and fault simulation.

Problems With LSSD

- Design rules imposed on designers --- no freedom to vary from the overall schemes, and higher design and hardware costs (4-20% more h/w & 4 extra pins).
- No asynchronous designs.
- Sequential routing of latches can introduce irregular structures.
- Faults changing combinational function to sequential may cause trouble, e.g., bridging, CMOS stuck-open.
- Slow test application; normal-speed testing is impossible.
- Not good for memory intensive designs.