Practice Problems on Fault Simulation

1. Find a counterexample to the following statement: "*In a combinational circuit, two stuck-at faults f and g are functionally equivalent if and only if they are always detected by the same tests*".
2. Show that when n faults are simulated without fault dropping, a parallel fault simulator on a w-bit word computer will run $(n+1)(w-1)/n$ times faster than a serial fault simulator.
3. Consider a parallel fault simulator implemented on a machine with 32-bit word sizes. For a given circuit, it is required to simulate 2000 faults with 500 test vectors. What will be the speedup achieved by the parallel fault simulator as compared to a serial fault simulator.
4. For the circuit shown in Figure 1, show a collapsed fault set for single stuck-at faults.
5. For the circuit shown in Figure 1, show steps of fault simulation using *parallel fault simulation* technique using the test vectors as shown, and identify the faults that get detected. Use the collapsed fault list for your calculation.
6. For the circuit shown in Figure 1, show steps of fault simulation using *deductive fault simulation* technique using the test vectors as shown, and identify the faults that get detected. Use the collapsed fault list computed in the previous problem for your calculation.
7. For the circuit shown in Figure 1, show steps of fault simulation using *concurrent fault simulation* technique using the test vectors as shown, and identify the faults that get detected. Use the collapsed fault list computed in the previous problem for your calculation.
8. For a 3-input gate whose input deductive fault lists are L_A, L_B and L_C respectively, compute the fault list of the output line F, for the following cases:
    a. Gate type is AND, and inputs are 1,1,1
    b. Gate type is AND, and inputs are 1,0,1
    c. Gate type is NOR, and inputs are 0,1,1
    d. Gate type is XOR, and inputs are 0,0,0
    e. Gate type is OR, and inputs are 0,0,0
9. For a 2-to-1 multiplexer with inputs A and B, select line S, and output F, compute the deductive fault list of F for the following cases:
    a. A=0, B=1, S=0
    b. A=0, B=1, S=1
    c. A=1, B=1, S=1

10. Is it possible to have a combinational circuit *C* with some signal line *S* and a test vector *T* such that *T* detects both *S/0* and *S/1* faults? Give an example if it is possible, or prove that it is impossible.

11. Find an example where two stuck-at faults *f* and *g* have a dominance relationship between them, but they are not faults on input or output lines of the same gate.

12. Prove that in a fanout-free circuit comprised only of primitive gates, fault collapsing can always be performed in such a manner that the only single stuck-at faults remaining in the target fault list are at the primary inputs of the circuit.

13. Consider single stuck-at faults *f*, *g* and *h* in a combinational circuit C. Given that fault *f* dominates *g*, and that *g* dominates *h*, prove that *f* dominates *h*.

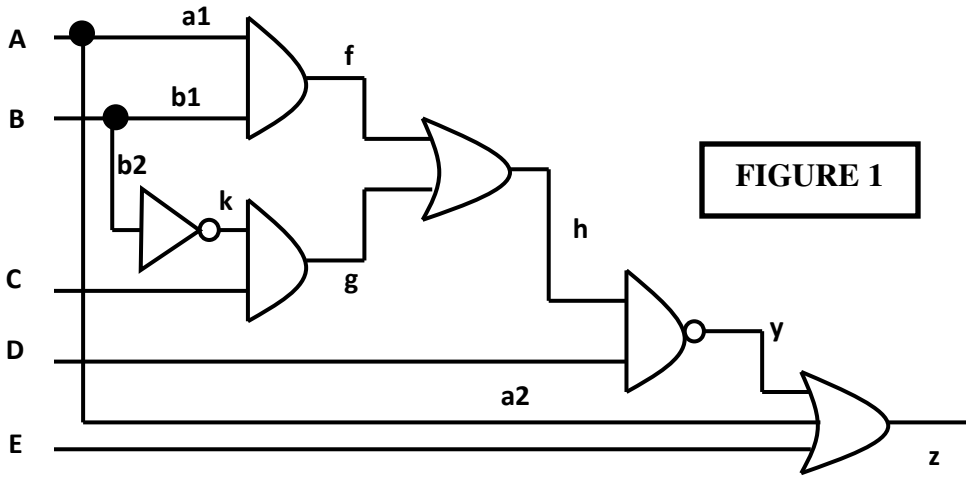

FIGURE 1

Test vector T1: A=0, B=0, C=1, D=1, E=0

Test vector T2: A=0, B=1, C=1, D=1, E=0

Test vector T3: A=1, B=1, C=0, D=1, E=0