Problems on Fault Modeling

1. Implement a full adder using AND, OR and NOT gates, and determine the total number of (i) single stuck-at faults, (ii) multiple stuck-at faults.

2. Generate a minimum set of test vectors to detect all single stuck-at faults for an \( n \)-bit parity checker implemented as a cascade of \((n-1)\) exclusive-OR gates. Repeat the exercise where each exclusive-OR gate is implemented by elementary logic gates (AND, OR, NAND, NOR, NOT).

3. For a 2-input CMOS NAND circuit:
   a. Find a two-pattern test for each single-transistor stuck-open fault.
   b. Rearrange the eight vectors in a compact set, and show that this set can be constructed from the single stuck-at faults tests for the NAND gate.
   c. For each stuck-at fault of the NAND gate, find an equivalent transistor (stuck-open, stuck-short or combination) fault.

4. Find the minimum number of test vectors required to test for all single stuck-at faults in the following circuits:
   a. A 289-input exclusive-OR gate
   b. A 76-input exclusive-OR gate
   c. A 12-input exclusive-NOR gate
   d. A 75-input exclusive-NOR gate
   e. An 8-input NAND gate
   f. A 6-input OR gate
   g. A full adder implemented using AND, OR and NOT gates
   h. An 8-bit parity generator constructed using 2-input exclusive-OR gates

5. Using functional fault modelling, determine the test sets for the following:
   a. A 8-line-to-1-line multiplexer
   b. A 3-to-8 decoder

6. The number of failures in \(10^9\) hours is a unit (abbreviated FITS) that is often used in reliability calculations. Calculate the MTBF for a system with 500 components where each component has a failure rate of 1000 FITS.

7. Use functional fault model to generate test sets to detect faults in the following:
   a. A 8-to-1 multiplexer
   b. A 2-to-4 decoder