Synchronous Sequential Circuits

Assignments

1. Show how will you carry out the following conversions:
    a. T flip-flop to S-R flip-flop
    b. T flip-flop to J-K flip-flop
    c. D flip-flop to T flip-flop
    d. D flip-flop to S-R flip-flop

2. Draw the gate-level schematic diagram of a S-R master-slave flip-flop, and hence explain how race condition occurs in the circuit.

3. Synthesize each of the following design descriptions into a synchronous sequential circuit, consisting of flip-flops and gates only. The choice of flip-flops to be used is mentioned along with the design descriptions.

    a. Design a serial magnitude comparator that takes two inputs X1 and X2, and produces three outputs LT (less than), GT (greater than) and EQ (equal). The bits x1(t) and x2(t) and fed in synchronism with a clock pulse, and the outputs are continuously updated on a clock-by-clock basis.
    [*Use D flip-flop, and J-K flip flop in two alternate implementations*]

    b. Design a serial bit converter that takes a binary number of arbitrary length as input, and outputs the corresponding 2's complement form. The inputs bits are fed LSB first.
    [*Use S-R flip-flop in the implementation*]

    c. Design a 4-bit BCD counter, that counts through 0000 to 1001 and then back to 0000. Make relevant assumptions where necessary.
    [*Use T flip-flop in the implementation*]

    d. Design a 5-bit counter that would count through the following sequence before repeating: 00011, 01110, 01000, 11000, 01010, 10101.
    [*Use J-K flip-flop in the implementation*]

    e. Design a 5-bit counter that would count through the following sequence before repeating: 00001, 00010, 00100, 01000, 10000.
    [*Use D flip-flop in the implementation*]