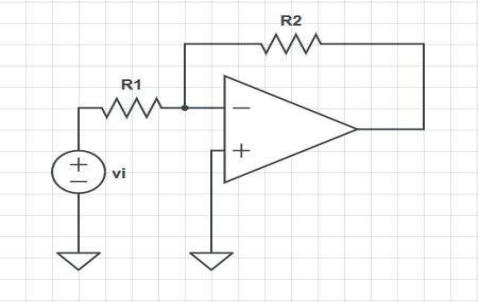
Tutorial Assignments: Analog Signal Processing (EE60032),

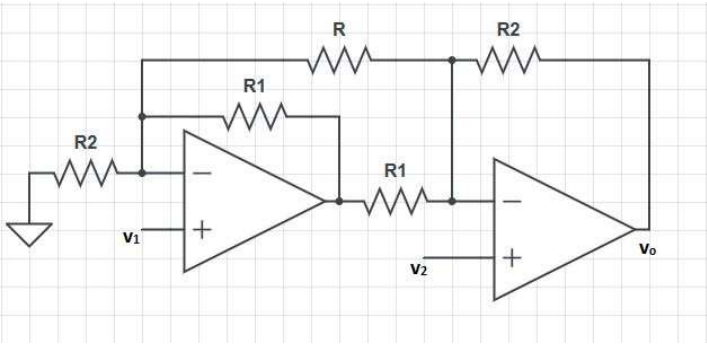
Department of Electrical Engineering, Indian Institute of Technology, Kharagpur

Faculty: Ashis Maity Session: Autumn 2018

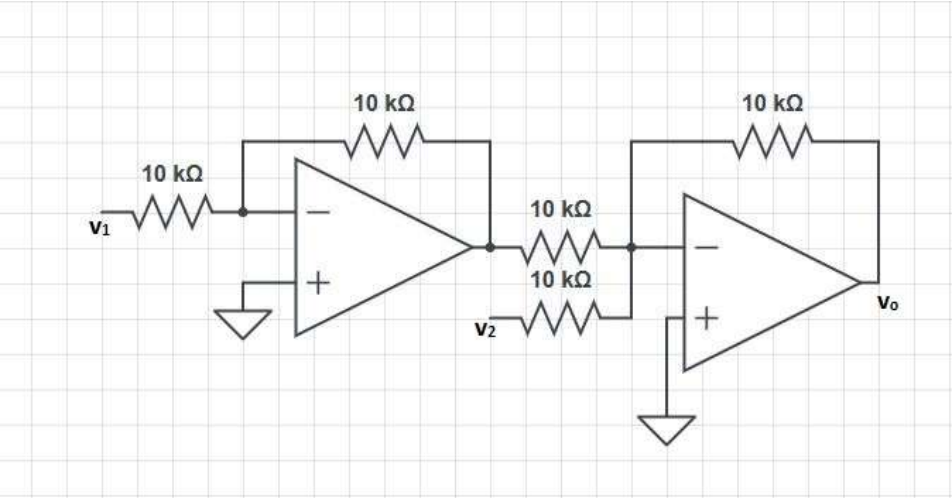
1. Design an inverting amplifier for a nominal gain of 4, a gain error of 0.1% and an input impedance of 10 kΩ.



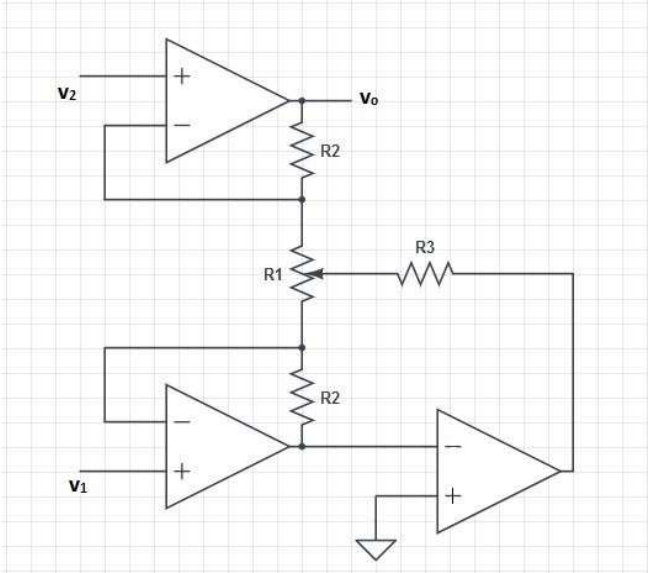
2. Design a circuit which can generate an output voltage $v_o=-2(3v_1+4v_2+2v_3)$, where v_1, v_2 and v_3 are the input voltages.
3. For the instrumentation amplifier shown in the figure below, verify that $v_o= (1+R_2/R_1+2R_2/R)(v_2-v_1)$.



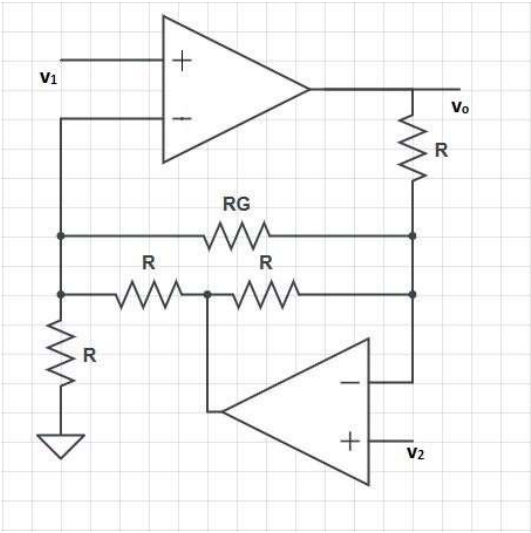
4. Calculate V_o for the circuit shown below for V_1=5V and V_2= 2V.



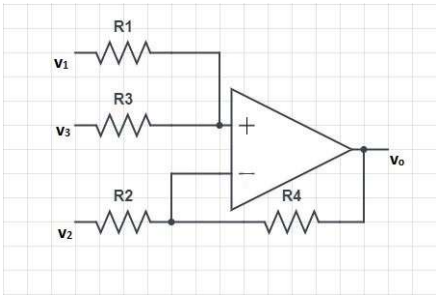
5. Compared with the classical triple op-amp, below figure uses fewer resistances. The wiper is nominally positioned halfway to maximize the CMRR. Show that
   $v_o = (1+2R_2/R_1)(v_2-v_1)$.



6. Show that $v_o = 2(1+R/R_G)(v_2-v_1)$.

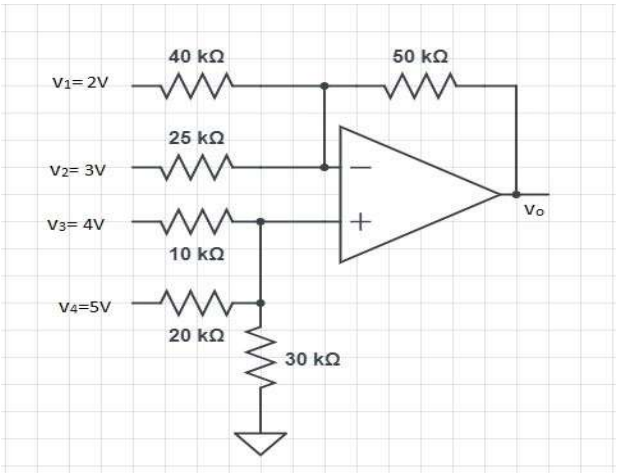


7. Show that $v_o = a_1v_1+a_2v_2+a_3v_3$. Find a_1, a_2 and a_3. Find the value of v_o if
   i) R_4 is shorted.
   ii) R_4 is removed.
   iii) R_1 is shorted.

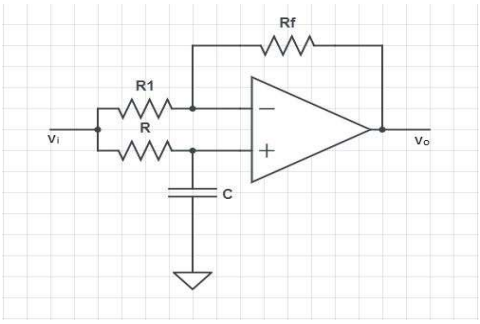


8. Design an adder circuit using op-amps to get v_o= - ($0.1v_1$+v_2+$10v_3$), where v_1, v_2 and v_3 are the inputs.

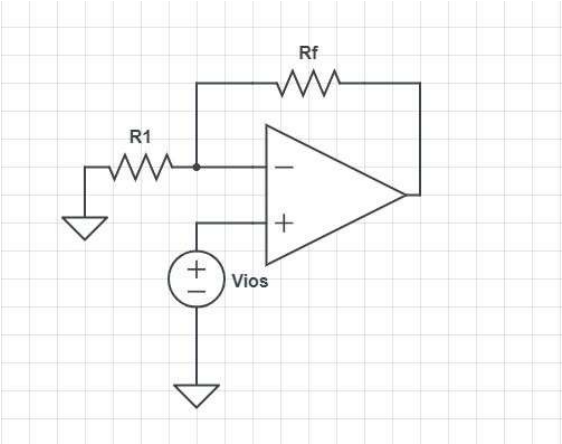
9. Find V_o.



10. Determine the phase angle and the time delay for the circuit shown in the figure for a frequency of 2 kHz. Given: R_1= 20 kΩ, R= 39 kΩ, R_f= R_1 and C= 1nF.



11. For a non-inverting amplifier, R1= 1 kΩ and R_f= 10 kΩ.
    a) Calculate the maximum output offset voltage due to v_{ios} and I_B where v_{ios}= 10mV, I_B= 300 nA and I_{OS}= 50 nA.
    b) Calculate the value of R_{comp} needed to reduce the effect of IB.
    c) Calculate the maximum offset voltage if R_{comp} is connected to the circuit.


Rf
R1
Vios