Cadence Analog Circuit Tutorial

Schematic Entry for Analog Designs- Passive Circuits (RLC Circuit) In this tutorial, we will build the circuit shown in figure 1 below, using the Cadence Composer tool.

Note: This example follows the example of University of Minnesota, Duluth.

1. Accessing Cadence Using Exceed Hummingbird Connectivity $9.0 \rightarrow Exceed \rightarrow Exceed XDMCP$ Broadcast Choose ees2 (129.118.19.10) **XDMCP Display Manager Chooser (20) XDMCP Display**

E<u>x</u>it <u>H</u>elp





2. Invoking the Command Interpreter Window (CIW) Find icfb file. It is located at /cadence/tools/dfII/bin/icfb

-	File Mana	iger – ees2:bin		•
<u>F</u> ile <u>S</u> elected <u></u>	<u>/</u> iew			<u>H</u> elp
	<u>x-x-x</u>]		
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/cadence/tools/	dfII/bin			
getSpectreFiles	hdldebug	hspice	icc2cdba	
icfb	jcfb.exe	i cms	icms.exe	
icmsBatch	jes3	jsc	ivremote	
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100 Items 1 Hidde	en			

Left double click icfb file to open CIW command interpreter window.

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mo	se L: M: R:		
>			

Select Tools \rightarrow Library Manager..... to open Library Manager.

🖻 📃 Library Manager	: WorkArea: /cadence/tools.	sun4v/dfII/bin 🛛 🗗							
<u>File E</u> dit <u>V</u> iew <u>D</u> esign Mar	lager	<u>H</u> elp							
🗆 Show Categories 📃 Show	v Files								
Library	- Cell	- View							
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- Messages		ĭ							

On the CIW banner, select File \rightarrow New \rightarrow Library In the New Library window, under Library type "mydefault"

-	New Library
- Library	
Name	mydefault
Directory	,
cadence local nsmail simulati	ion
/export	/home2/hej
— Design I	Manager
Use)	TONE
O Use N	o DM
ОК	Apply Cancel Help

Click OK button. In the Technology File window, choose "Don't need a tech file".



3. Creating a New Design

Select File \rightarrow New \rightarrow Cellview from the CIW, and fill in the form as below to define the new schematic cellview.

In the Cell Name field, type RLC_Filter_Circuit.

In the Tool selection, select Composer-Schematic which automatically defines the View Name to schematic.

Click OK.

-	Crea	te New F	ile									
OK Cancel Defaults Help												
Library Name mydefault =												
Cell Name	e R	RLC_Filter_Circuid										
View Nan	ne s	schematič										
Tool	C	omposer-S	Schematic =									
Library p	Library path file											
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An empty Window appears as next figure.

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4. Schematic Capture

4.1 Placing the Intances

Click on the Instance Icon and then click the Browse button in the form to open Libraries browse window.

Select the following:

Under the Library column, select analogLib.

Under Cell, select res.

Under View, select symbol

🗖 Libr	ary Browser – Add Insta	nce 🔽 🗖
Show Categories		
- Library	Cell	- View
janalogLib	ľres	jsymbol
NCSU_analog_parts NCSU_digital US_8ths ahdlLib analogLib basic cdsDefTechLib functional mydefault pCells rfExamples	> pvcvs pvcvs2 pvcvs3 res scasubckt scccs sccvs schttky scr spltswitch spltswitch spltswitch	ams auCdl auLvs cdsSpice hpmns hspiceS libra mharm spectre syectres symbol
Close	Filters	Help

Edit the Add Instance form by modifying the Resistance value to 22K Ohms, as shown below if Resistance value is not 22K Ohms.

-		A	dd Instai	nce		
Hide	Cancel	Defaults				Help
Library Cell	analogL reš svmboli	ib			Brow	se
Names Array	Ĭ	Rows	1į́	Columns	lĭ	
Rotat	e	Si	deways		Upside Do	wn
Resistan Tempera	ce ture coeff	icient 1	22 k Ohm	8		
Temperat Model na	ture coeff me	icient 2	I.			
Length			¥			

Click in the composer window to place the resistor.

Add the other instances symbols from the analoglib as indicated below:

C (analoglib, cap) = 47n F

L (analoglib, ind) = 500m H

R (analoglib, res) = 75 ohm

Ground (analoglib, gnd)

Click on Cancel.

4.2 Adding the I/O Pins

In the lower left side of the Composer window click on the Pin icon. Add the input and output pins, shown as following.

Under Pin Names, type Vin or Vout. Note that Direction in the form reads input or output.

-			Add Pin	
Hide	Cancel	Defaults		Help
Pin Name	s	Vin		
Direction		input	Bus Expansion	n 🖲 off 🔵 on
Usage		schematic r	Placement	singlemultiple
Rotate	e		Sideways	Upside Down

4.3 Connecting Wires

Click on the icon Wire (narrow) to connect wires,

Click two ends the wire to be connected to connect a wire between these two ends. Wire the components as show below.

	1	4	1	14	82	84	25	23	. 2	<u>د</u> .	93	13	52	123	32	2	2	82	84	81	82	352	25	8		53	23	$\overline{\mathcal{D}}$	52
3	1	12			1	1	82	14	ي ا	V .	\$3	S		25	32		3	8		85	53	52	82	10	50	13	8	25	35
3	52	1	÷	8	. 53	535	52	-	·A	AN			125	12	32	12	13	8		535	335	53	52	53	<u>.</u> :	1	5	12	12
8	Vîn					8	10	•	-1	/.V	V.		33		8			*		8	1	10	•	_			>	/ou	t ·
8		15	1	-	8	8	10	:8	8	85		10	33		8	12		24		18	12	10	-	8	15	•	10		3
			13	33	12	22	53	53	12	12			8		33	\sim			4	R1.	<u></u>	122	-					æ	8
							63	0		13			92					V.	5	r=7	5	-	-		•				÷
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*		3	2	1	1.5	1.1	80	•	8			=4	7n		1	3		1	28			-80	-	20	20	*	20	*	*
3				28	1	19	80	60	80		~		- U	30				2	- 22	24	1	80	÷0	25				33	3
3			12	14	52	55	88	23		-		1	35	3	2			14	2	84	33	20	23					3	3
12			1	22	52	15	23	28		18			35	5	12	1	1		La	LØ.		23	28	\tilde{k}				35	33
3		N.	53	8	12	84	23	23	12	28	78	70	32	22	5	12	12	3	3.	I=5	00m	23	23			70	10	22	22
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33	1	52	20	85	555	105	52	52	50	<u>\$</u> \$	53	63	25	25	32	1	1	88	81	13			82	35	<u>88</u>	53	53	25	2
3		82	33	-	8	10	10	:	8	8	10		35		8	82	12	33	1	• ·	12	128	13	23	15				
8		12	-	82	83	8	10	-	8	69	11		33	.75	83	12	11	33	12	g	nd.							3	33
				-		-						-	w.	a.				-	1	V.					x 11			a.	w.

4.5 Checking and Saving

Click on the design icon Check and Save to check and save the schematic. If Warning/Errors appear, check schematic and fix the problem as necessary. Warnings are not as crucial as Errors.

Repeat until no Errors.

5. Creating the Symbol Cellview

Create a symbol (black box) to represent our circuit. From schematic view go Design \rightarrow Create Cellview \rightarrow From Cellview.

A window as below appears.

-		Ce	Ilview From Cellview		1
ок	Cancel	Defaults Ap	ply		Help
Library N	lame	mydefaul∜			Browse
Cell Nam	e	RLC_Filter_C	ircuit		
From Vie	w Name	schematic =	To View Name	symbol	
			Tool / Data Type	Compose	er-Symbol 🗖
Display (Cellview				
Edit Opti	ons				

Under Too/Data Type, select Composer-Symbol.

A new Composer-Symbol Editing window appears.



6. Creating the TestFixture (testbench)

Create a new schematic cell using the above circuit symbol as one of its instances. In Cadence CIW, choose: File \rightarrow New \rightarrow Cellview...

Creating a new Cell called Test_RLC_Filter_Circuit and fill it as shown below,

-		Create	New File	
ок	Cancel	Defaults		Help
Library N	ame 🗌	mydefa	ult 📼	
Cell Name	, Г	est_RLC_F	ilter_Circu	
View Nan	ne s	chematič		
Tool	C	omposer-S	chematic 🗆	
Library pa	ath file			
/export/	home2/h	e∕cds.libį̇́		

Click OK to open a new Composer-Schematic window.

Add components according to the following table, and wire those components as figure below.

rabie rab o miter test	en cuit componento		
Library Name	Cell Name	View Name	Properies/Comments
mydefault	RLC_Filter_Circuit	Symbol	N/A
analogLib	Vsin	Symbol	AC Magnitude=1
			Amplitude=50m
			Frequency=1M
			Offset Voltage=0
analogLib	Сар	Symbol	Capacitance=1p
analogLib	Gnd	Symbol	N/A

Table RLC filter test circuit components

19	54 - 54	194	194	19	-										-10	1.	36	16	16	38
×	_		n	et3		vin		×	×			×	V	out	Ē	net	6		_	
38	1 .		18		L											3		×		
	T VØ		36		8		×			\mathbf{x}			18	3	8		38	×	1	
\sim (€ vo	o=0 o=5	Øm		58		33	×				×			×		×		T	CØ
	_ fr	eq=	1M	18	18	18	×			\mathbf{x}			×	15	8		18	3	T	
34	T ·		18		×		8	\mathbf{x}	\mathbf{x}	\mathbf{x}	\mathbf{x}	\mathbf{x}	×	15	8	$\left \cdot \right $	\sim	×	1	
		×	×	5	18	5	×	\mathbf{x}	\sim		×	×	×	5	8	\mathbf{x}	×	×.	T	
38			38	38	5	38	34							38	8		18			
38			38	3	38	14	3													
34			56	16	38	14	×	×	×	×		16	×	38	8	3	5		×	
			×	×.	16	÷.					-		1	5	8		36	×	×	
					×		×	×	×		\downarrow	gna	×		×		×	×	×	

8. Initializing the Simulation Environment

Open Test_RLC_Filter_Circuit schematic if it is closed.

In the schematic window, select Tools \rightarrow Analog Environment. The window appears as shown below.

🗖 📃 Affirma	Analog Circuit Design Environment (1)	•
Status: Ready	T=27 C Simulator: spectr	e 4
Session Setup Analyses	Variables Outputs Simulation Results Tools	Help
Design	Analyses	∽₹_₽
Library mydefault	# Type Arguments Enable	⇒ AC = TRAN ⇒ DC
Cell Test_RLC_Filter_C		¦ x v z
Design Variables	Outputs	[‡ ′
# Name Value	# Name/Signal/Expr Value Plot Save March	
		8
		8
>		\sim

The icons on the right provide quick access to frequent commands/menus.

9. Choosing a Simulation Engine

In the Simulation window, select Setup \rightarrow Simulator/Directory/Host...

Choose the Simulator cyclic field is reading **SpectreS**

Keep Project Directory to as default. This creates a new directory under use's cadence folder.

- Choo:	sing Simi	ulator/D	irectory/Host Affirma Analog Circuit	Desi
ок	Cancel	Defaults		Help
Simulator	r	spectre S	=	
Project D	irectory	~/simul	ation	
Host Mod	le	local (remote 🔿 distributed	
Høst				
Remote t	Prectory			

Note: If the simulator cdsSpice is chosen, the setup procedure is the same as SpectreS. If the simulator Spectre is chosen, the setup is different from SpectreS and the details will be shown in Appendix.

10. Choosing the Analyses

In the Affirma Analog Circuit Design Environment window, click Analysis \rightarrow Choose pull down menu to open the analyses window.

Several analyses modes are set up.

10.1 Transient Analysis

In the Analysis Section, select tran and set the Stop Time field to 3u. Before Click APPLY button, turn on the Enabled field (hidden by the lower left corner).

- Cho	osing A	nalyses	Affi	rma Anal	log Circuit Desi	ign En
ок	Cancel	Defaults	s Apply			Help
Analy	sis	tran	ac	⊖sp	Opdisto Osp	SS
)dc	⊖xf	Opss	Onoise	
		_				
		T	ransient	Analysis		
Stop	Time	3પ્				
Accu	racy Def	aults (en	rpreset)			
	conserva	ative 🗌	moderate	e 🔲 liberal		
Enabl	ed 🗌				Options	i

10.2 AC Analysis

In the Analysis Section, select ac (refer to next figure). Set the Sweep Variable to Frequency, the Sweep Range to Start-Stop, (Start: 0.01k, Stop: 10k) and set the Sweep Type to Logarithmic Per Decade. Turn on the Enabled field before click on Apply.

🖳 Choosing Analyses —— Affirma Analog Cire	cuit Design En
OK Cancel Defaults Apply	Help
Analysis tran 🔵 ac 🔿 sp 🗇 pdi	sto Ospss
Cdc Cxf Opss Choi:	se
AC Analysis	
Sweep Variable	
Frequency	
Temperature	
Component Parameter	
Model Parameter	
Sweep Range	
Start-Stop Start 0.011 Stop	10kj
Center-Span	
Sweep Type	
Logarithmic Points Per Decade	20
Total Points	
Add Specific Points 🗌	
Enabled	Options

10.3 DC Sweep and DC Operating Point

In the Analysis Section, select dc. In the Sweep Variable section, select Component Parameter. Click on Select Component and the supply source from the Schematic window. A form appears listing all the instances parameters. In it select the dc parameter. Click OK. In the Sweep Range section, select Start-Stop. (Start: 0, Stop:100). Turn on the enable when it is done, the form should appear as shown next.

🖻 Choosing Analyse	s — Affi	irma Anal	log Circ	uit Desig	n En
OK Cancel Default	s Apply			Ī	Help
Analysis 🔿 tran	Cac	Osp	Opdis	to Ospss	
e dc	⊖xf	Opss	Onois	e	
	DC Ana	dysis			
Save DC Operating P	oint 🗌				
Sweep Variable	_		. 🗖	чđ	_
Temperature	0	omponent f	Name 🔽	۰ų	
Component Parar	neter _	Sele	ect Comp	onent	
Model Parameter	P	arameter N	ame d	9	
Sweep Range					
🔵 Start-Stop	Start Ű		Ston	100	
Center-Span			Jup		
Sweep Type					
Automatic 🗖					
Add Specific Points					
Enabled				Options	•

The final look of the Affirma Analog Circuit Design Environment window should be as shown below.

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S	tatu	s: Ready	/						T=27 C	Simulator	: spectre:	S 8
Ses	sion	Setup	Analyses	Varia	bles	Outputs	Simu	lation	Results	Tools		Help
		Desig	n					Analy	ses			Ł
Libra	ary	mydefau	lt	#	Тур	e .	Argum	ents	• • • • • • •	• • • • • • • • • •	Enable	⊐ AC ⊏ TRAN
Cell		Test_RL	.C_Filter_	1	tra	n	0 10	3u 10r	20	Loga	yes wee	⇒DC
Viev	v	schemat	ic.	3	dc		10	0	100		yes	Ϊ ူ Ϊ x y z
	De	sign Var	iables					Outp	uts			∎ ŧ ľ
#	Nan	le V	/alue	#	Nam	e/Signal	/Expr	Ţ	Value	Plot Save	March	
												~
												}
>												\sim

11. Saving and Plotting Simulation Data

Select Output \rightarrow To be Plotted \rightarrow Select on Schematic to select nodes to be plotted. By clicking on the wire on the schematic window to select voltage node, and by clicking on the terminals to select currents. Select the input and output wires in the circuit. Observe the simulation window as the wires get added.

12. Running the Simulation – The Waveform Window

Click on the **Run Simulation** icon.

When it complete, the plots are shown automatically.

We'll next modify the appearance of the displayed waveforms as following figure.



13. Exiting

Close every window.

Right click desktop, a menu pops up as next. Then click log out to exit.

Workspace Menu	
Applications	
Cards	Þ
Files	D.
Folders	
Help	Þ
Hosts	D.
Links	
Mail	P.
Tools	
Windows	D.
🔄 Add Item to Menu	
🖬 Customize Menu	
🖀 Lock Display	
🙈 Suspend System	
🕅 Log out	

Appendix

Simulation using Spectre

1. Choosing the Simulator

After reaching the step 9 in the tutorial you have to choose a simulator for simulating the circuit. In the tutorial we showed the set up for SpectreS simulator. If you want to use Spectre instead of SpectreS select Spectre in the command window as shown below.

	8	19	8	12	50	20	125	12		8	23	8	8	12	-		8	12	15	.75	83	10		85
3	1		100	13	10			50	N.		RI	C	Fill	er	10		Ni.	1	30		- 1	10	3	\mathcal{A}
82	ļ		82	8	26		82	<u>.</u>	VI	٩.		~			23	10	VO	ut	24	12	1		20	N.
1	1	50	3	1	12		12	1	5	32	8	53	35	12	12	-8	3	53	50		81		5	1
5	82	1	\sim		53	2		12	0	3	12	12	2		53		\sim	8			2			
1	191			1	20	35		83			12		3		10		2	55	15		3			
2	83		12	8	25			82	13	12	1	18	33	2	83	13		82	22		34 1		93	
	1	8	8	22	10			8	* 1	8	8	5	3		10		8	12	8	ne	et16	• c	Ø	
3	24		18	2	43	$\langle \mathbf{x} \rangle$	3	14	30	38	\sim	\mathbf{x}_{i}	$\left \mathbf{x} \right $		•	×	\mathbf{x}	24	\mathbb{R}^{2}	$\langle \mathbf{x} \rangle$	3 -	Ļ,	c:1	p.
52	14		82	8	22	2	N.	14	2	52	53		22	52	23	70	5	83		2	. 1	T	1	14
1	33	10	32	81	8	25	1	55	8	32	1	5	35	32	12	13	2	53	50	. 9	gnd!	•	5	<u>ي</u>
×		ĸ	8	13	10	÷	$^{\prime\prime}$	-			3	83	\sim	÷	83	8	\sim	-	83	×	38		35	\mathcal{F}
	10			1	23	5		83		3	14		3		2		1	84		5	5			4
2	83	88		82	25		4	22	8	32	82	10	32	8		gi	nd	702	10	32	3	_	13	
	8	20	\otimes	10	53	87		22	*	33	19	10			2	7		82	18	æ	10	52		\cdot
3			5	\sim	•	÷	3	124	8	5	4		\sim			×	\sim	24		a.	2	-	8	



Choosing Spectre as the Simulator

2. Setting up the Analog Stimuli

After selecting the simulator we need to set up the analog stimuli. For doing this we go Setup \rightarrow Stimuli \rightarrow and fill out the settings as shown in the Figure below.

-			Setu	p Analos	g Stii	muli		
ок	Cancel	Apply						Help
Stimulu	ıs Type	🔘 Inp	uts () Global :	Sourc	es		
ON I	/gnd!	Voltage	e sin	e "AC ma	gnitu	ide"=1		
				Change				
Enabled	1 🖬	Fund	ction	sin 🗆		Туре	Voltage =	
AC mag	jnitude			1				
AC pha	se			Ĭ				
DC vol	tage			Ĭ.				
Offset	voltage			0 <u>ř</u>				
Amplitu	ide			50m <u>í</u>				
Freque	ncy			1M <u></u>				
Delay t	ime							
Dampin	ig factor							
Source	type			sine				
XF mag	pitude							
PAC ma	agnitude							
PAC ph	ase							
Initial p	hase for	Sinusoi	id					

3. Transient Analysis

In this appendix we will show only the transient analysis. The set up for DC and AC analysis is same as for the SpectreS simulator which is described in the tutorial.

1. In the Analysis Section, select tran.

2. Set the Stop Time field to 3u.

3. Turn on the Enabled field (hidden by the lower left corner).

4. Click APPLY. (do not click OK)

Notice that in the Affirma Analog Circuit Design Environment Window, under the Analysis Section, a line was listed to describe this analysis.

Choosing Analyses Affirma Analog Circ	uit Design En
OK Cancel Defaults Apply	Help
Analysis 🔵 tran 🔿 ac 🔿 sp 🔿 pdis	to ()spss
dc xf pss nois	e
Transient Analysis	
Stop Time 34	
Accuracy Defaults (empreset)	
🗌 conservative 🔄 moderate 📃 liberal	
Enabled	Options

4. Saving and Plotting Simulation Data

The simulation environment is configured to save all node voltages in the design by default. You can modify the default to save all terminal currents also, or you can select specific set of nodes to save. We'll select these nodes from the schematic window. Select Output \rightarrow To be Plotted \rightarrow Select on Schematic.

Node voltages can be selected by clicking on the wire on the schematic window, and currents by clicking on the terminals. Unselecting can be performed either by clicking on the terminal/node again, or by selecting the corresponding line in the Outputs section of the Simulation window and clicking on the Delete icon. Select the input and output wires to the circuit. Observe the simulation window as the wires get added.

The final look of Affirma Analog Simulator is shown below

🗖 🗌 Affirma	Analog Circuit Design Environment (1)	• 🗆
Status: Selecting outputs to be plotted T=27 C Simulator: spectre		
Session Setup Analyses	Variables Outputs Simulation Results Tools	Help
Design	Analyses	r,₹
Library mydefault	# Type Arguments Enable	⊐ AC ⊏ TRAN
Cell Test_RLC_Filter_C	1 tran 0 3u yes	⊐ DC
View schematic		T T T x Y Z
Design Variables	Outputs	Œ,
# Name Value	# Name/Signal/Expr Value Plot Save March	
	1 I yes allv no	<u> </u>
	2 net16 yes allv no	
		畿
> Select on Schematic Outp	its to Be Plotted	\sim

5. Running the Simulation

To run the simulation click Simlation \rightarrow Run. The following graph will be plotted.



Reference

1) Shaer, Bassam, University of Minnesota, Duluth http://www.d.umn.edu/~bshaer/cadence/AnalogTutorials/Passive_Circuit_Cadence_Tuto rial.htm